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ECAT SINGLE EUROCARD PC COMPATIBLE COMPUTER

USERS' MANUAL

V1.0 7 JULY 1990

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ECAT MANUAL V1.0 ERRATA AND ADDENDUM

Please note the following changes and additions to the manual:

Page 5, between paragraphs 7 and 8, add the following text:

> Some disk drives do not have a correctly mating cut-out to match the polarising bump on the 34 way female ribbon cable connector. In fact, some disk drives even have a cut-out on the wrong side, to encourage you to plug the cable in the wrong way around. Be very careful to match pin 1 on the cable with pin 1 on the disk drives. (If the cable is plugged in the wrong way around the disk drive activity LED will be on permanently).

Page 23, between paragraphs 1 and 2, add the same text as was added on page 5.

Page 29, paragraph 5:

Change "ECATADR7" to "ECATADRY".

Page B2, between paragraphs 2 and 3, add the following text:

Both R6 and R7 are 1k ohm.

Page E3 change the table headed IC12 MEMORY DEVICE to read:

IC12 MEMORY DEVICE	FIT LINKS TO E3 AS FOLLOWS:
32k byte EPROM	A8-A9 and B8-B9
64k byte EPROM	A8-A9 and B7-B8
128k byte EPROM	A7-A8, A9-A10 and B7-B8
256k byte EPROM	A7-A8, A9-A10 and B7-B8
512k byte EPROM (1)	A7-A8, A10-B10 and B7-B8
512k byte EPROM (2)	A7-A8, A11-B11 and B7-B8

(1) assumes EPROM occupies a single 512k byte block
(2) assumes EPROM occupies two discontiguous 256k byte blocks

Page F6, Table F5, change two lines to read:

7	GND	8	8
8	BLUE	3	3

REV C PRINTED CIRCUIT BOARD

The REV C version of the PCB has introduced a number of slight enhancements - the reset switch is more accessible, tracking errors have been corrected, pins added to E3 to allow the use of 4M bit EPROMs, rechargeable Nicad battery and improved DMA operation.

A new manual will shortly be produced providing full documentation of these features. In the meantime please call DSP Design if you need clarification of any of the above enhancements.

ECAT SINGLE EUROCARD PERSONAL COMPUTER

USERS' MANUAL

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1 INTRODUCTION

The ECAT (Eurocard AT Compatible Computer) from DSP Design is one of a family of computers bringing an unprecedented level of minaturisation to PC compatible computing.

All of the electronics for an IBM AT compatible computer have been squeezed onto a single Eurocard circuit board, measuring just 100mm x 160mm. The ECAT can be used stand-alone, or as a processor card in an STEbus or PC bus computer. That this has been achieved is a tribute to the skill of DSP Design's engineers, and to the manufacturers of today's advanced integrated circuits.

An optional add-on board called the ECAT-X adds further features.

The ECAT brings new opportunities to designers of instrumentation, control systems and data acquisition systems - opportunities for greater minaturisation, improved reliability and reduced costs.

Other members of the ECAT family include the ECPC, a lower cost PC compatible computer, and the ECPC-LCD which drives LCD displays.

1.1 ECAT FEATURES

The ECAT offers you:

- Emulation of IBM PS/2 Model 30 (similar to the IBM AT).
- 80286 processor running at 12.5MHz or 16MHz.
- 512k, 1M, 2M or 4M of DRAM on board.
- Runs almost all MS-DOS software written for the IBM PC/AT computers.
- PC compatible BIOS running MS-DOS, which can reside in the same EPROM as on-board ROM disk (strictly speaking the BIOS is PS/2 Model 30 compatible).
- Floppy disk controller for two 3.5" and 5.25" drives.
- CGA, Mono and Hercules graphics (EGA, VGA with the addition of the ECAT-X board; plasma, electro-luminescent, LCD also available - ask).
- Keyboard input, sound output, RS-232 serial and Centronics printer ports.
- Two sockets for EPROM or SRAM (can be used for ROM and RAM disks) - more ROM disk space on ECAT-X.
- Battery backed-up calendar/clock chip.
- Operates stand-alone from +5V supply - very low power.
- ECAT-X board adds VGA or EGA graphics, 80287 maths coprocessor socket, second serial port, extra ROM disk.
- CMOS construction offers low power consumption and optionally extended temperature range operation.
- Expansion to other memory and I/O through powerful

STEbus (IEEE 1000) interface.
- Expansion to the popular PC bus with the ECAT-PC version.
- Two DMA channels for STEbus or PC bus transfers.
- Vectored and non-vectored interrupts.
- Board can be de-populated for target applications.
- Large range of industrial I/O available.

1.2 ECAT BENEFITS

The ECAT allows you to:

- retain PC/AT software while upgrading to improved mechanical format.
- run MS-DOS software from ROM and RAM disks - no mechanical disk drives required.
- reduce power supply cost and complexity.
- use ruggedised, standardised industrial racking and packaging.
- reduce the size of your system.
- operate stand-alone with a single-board AT.
- upgrade from existing STEbus PCs to much higher performance.
- expand your system using a wide range of I/O cards based on an international standard (STEbus, IEEE1000) or the popular PC bus.
- achieve greatly reduced development costs by using standard PC/AT software and development systems.
- provides upgrade path from DSP Design's ECPC single Eurocard PC compatible.

1.3 PC/AT COMPATIBILITY

The ECAT offers an extremely high degree of compatibility with IBM PC family of computers. This compatibility extends from the MS-DOS level, through BIOS-level compatibility to register-level compatibility.

The 80286 processor used on the ECAT board is supported by the Chips and Technologies Genie chip. The Genie includes on-chip peripherals - timers, interrupt controller, DMA controller etc - which appear to the programmer as identical to the equivalent Intel peripheral chips used on the original IBM PC and AT. The fact that these peripherals are identical to the Intel chips ensures compatibility not just at the BIOS level, but also at the register level.

In addition to the I/O resources in the Genie the chip provides other features. A keyboard and a loudspeaker port are included, and the chip looks after clock generation, address decoding, maths coprocessor support, expansion bus timing, EMS memory mapping and various other functions.

Around the Genie chip DSP Design have added a floppy disk controller and a multi-mode video graphics controller which again are identical to the corresponding components used on the IBM PC/AT. The disk controller will read and write 360k and 1.2M byte 5.25" floppies, as well as 720k and the high capacity 1.44M byte 3.5" floppy disks. All of these are standard PC formats. The video controller can operate in several PC-compatible modes. First there is the IBM monochrome alphanumeric mode (80x25 characters). Then comes Hercules compatible monochrome graphics (720x348 pixels). Next is IBM CGA colour graphics (640x200 pixels and 80x25 characters). Finally, there is a double scan CGA mode, which gives a better appearance to the CGA colour graphics.

And finally, an add-on board provides further AT compatible functions - EGA and VGA graphics, a second serial port, a maths coprocessor socket and space for a large ROM disk.

The user should take note however that the ECAT departs from IBM AT compatibility in some respects. This is because the Genie chip is actually IBM PS/2 Model 30 compatible rather than IBM AT compatible. The differences between a Model 30 with an 80286 processor and an AT are small. They relate mainly to differences in the keyboard controller and calendar clock chip, as well as a few registers relating to non-maskable interrupts and power-on configuration functions. The main difference that users are likely to encounter is that the ECAT will not run most software which uses the 80286 protected mode of operation. This includes the Xenix operating system.

DSP Design will be pleased to answer any questions that you may have with respect to the compatibility issue, however experiance so far indicates that incompatibility problems are rare and usually easily resolved.

1.4 STEbus AS A PC EXPANSION BUS

Users can operate the ECAT as a single board computer, or if expansion is required I/O boards can be accessed via the STEbus interface provided on the ECAT. (For users who want to use IBM PC bus expansion boards, a version of the ECAT is available which supports PC bus boards.)

The STEbus is an international standard, known as IEEE1000. An overview of the STEbus is provided in the Appendix G. The signals on the STEbus are very similar to those found on the IBM PC expansion bus - both buses have an 8-bit data bus, a 20-bit address bus, and interrupt and DMA request lines. DSP Design and other STEbus manufacturers have on offer a wide range of I/O boards which will work with the ECAT, in the same manner that a conventional PC can be enhanced by the addition of PC add-on boards.

The STEbus I/O card range includes analog and digital I/O cards, serial comms and local area network boards, stepper and servo motor controllers and other specialist functions. DSP Design has a full range of these boards, many of them available as all-CMOS extended temperature range designs.

It is the policy of DSP Design to introduce, where appropriate, new STEbus I/O cards which are software compatible with similar cards for the IBM PC. This has the tremendous advantage of allowing users to make use of the software which has already been written for the IBM PC cards. Take three examples. A BT approved Hayes compatible modem card works with the full range of MS-DOS communications programs. An Arcnet LAN card is compatible with popular PC LAN cards, allowing the ECAT to be networked with Novell Netware and other network operating systems. DSP Design's IEEE488 card will be compatible with the popular National Instruments card, allowing immediate access to MS-DOS data capture, graphical and data analysis software.

1.5 THE ECAT ARCHITECTURE

The block diagram in Figure 1 shows the architecture of the ECAT. The 80286 processor accesses local DRAM and EPROM memory; address decoding is very flexible and performed in a PAL device which can be changed if a different memory map is required.

The Genie chip performs a range of house-keeping and glue logic functions, as well as providing timer, interrupt, DMA, speaker and keyboard facilities. Connected to the internal buses are the floppy disk controller, a serial and parallel I/O chip, a calendar/clock chip and the video graphics chip which has its own memory-mapped video RAM.

Finally an STEbus (or PC bus) interface allows the ECAT to perform memory and I/O accesses to the STEbus (or PC bus). The Genie interrupt and DMA controllers are used by the on-board peripherals as well as being connected to the expansion bus.

1.6 GETTING STARTED QUICKLY

This manual gives all of the information that most users will need to have in order to operate the ECAT. Those people who need to write their own MS-DOS device drivers, or modify the BIOS, or who have special requirements may require further information. If this is the case our support engineers will be pleased to help you.

Most users will find getting started with the ECAT

simplicity itself. Those of you who can't wait to read the whole manual just follow these simple instructions...

First, provide a power source for the ECAT. Don't switch on the power yet. Power can be applied by plugging the ECAT into an STEbus or (PC bus) backplane, or by connecting it to a Powerterm board from DSP Design (the Powerterm is a small PCB with screw terminals and a small power supply circuit - regulated DC, unregulated DC or AC can be used). The ECAT draws around 580mA from a single +5V supply - and just 350mA if a CMOS 80C286 processor is fitted! Users may find DSP Design's Powerplane product - a combination of power supply and backplane - useful for development work.

Next, connect the cable assembly to the J2 connector. The ECAT-BP cable assembly allows connection of an AT keyboard, video monitor, printer, and serial device, as well as a 3.5" floppy disk drive.

Connect a monochrome or multi-scan monitor to the video connector (the 9-way female D-type connector) and an AT (not XT) keyboard to the keyboard connector (note that the keyboard must support Scan Code Set 1 - see section 3.3).

You can switch on your ECAT at this stage. You should see the BIOS EPROM run through a series of tests, and attempt to load MS-DOS from a floppy disk. It will of course fail to do this, and let you know by producing a sound on the loud speaker.

Switch off the ECAT and add a disk drive to the ECAT. The 34 way connector on the ECAT cable assembly plugs directly onto a 3.5" floppy disk drive - make sure pin 1 of the cable connector matches pin 1 of disk drive connector (with some drives the polarising bump on the cable connector may have to be cut off). Suitable disk drives are described in section 4.3.

Add a power supply cable to the floppy disk drive. Drives with a +5V only supply requirement can be powered through the Molex connector on the ECAT cable. Make sure that you connect the power connector the right way around - in the correct orientation the connectors will mate easily.

Power on the ECAT and disk drive, and insert an MS-DOS boot disk in the floppy drive. The ECAT should load MS-DOS and you will see the familiar MS-DOS sign on messages - now you can explore the power of the ECAT for yourself.

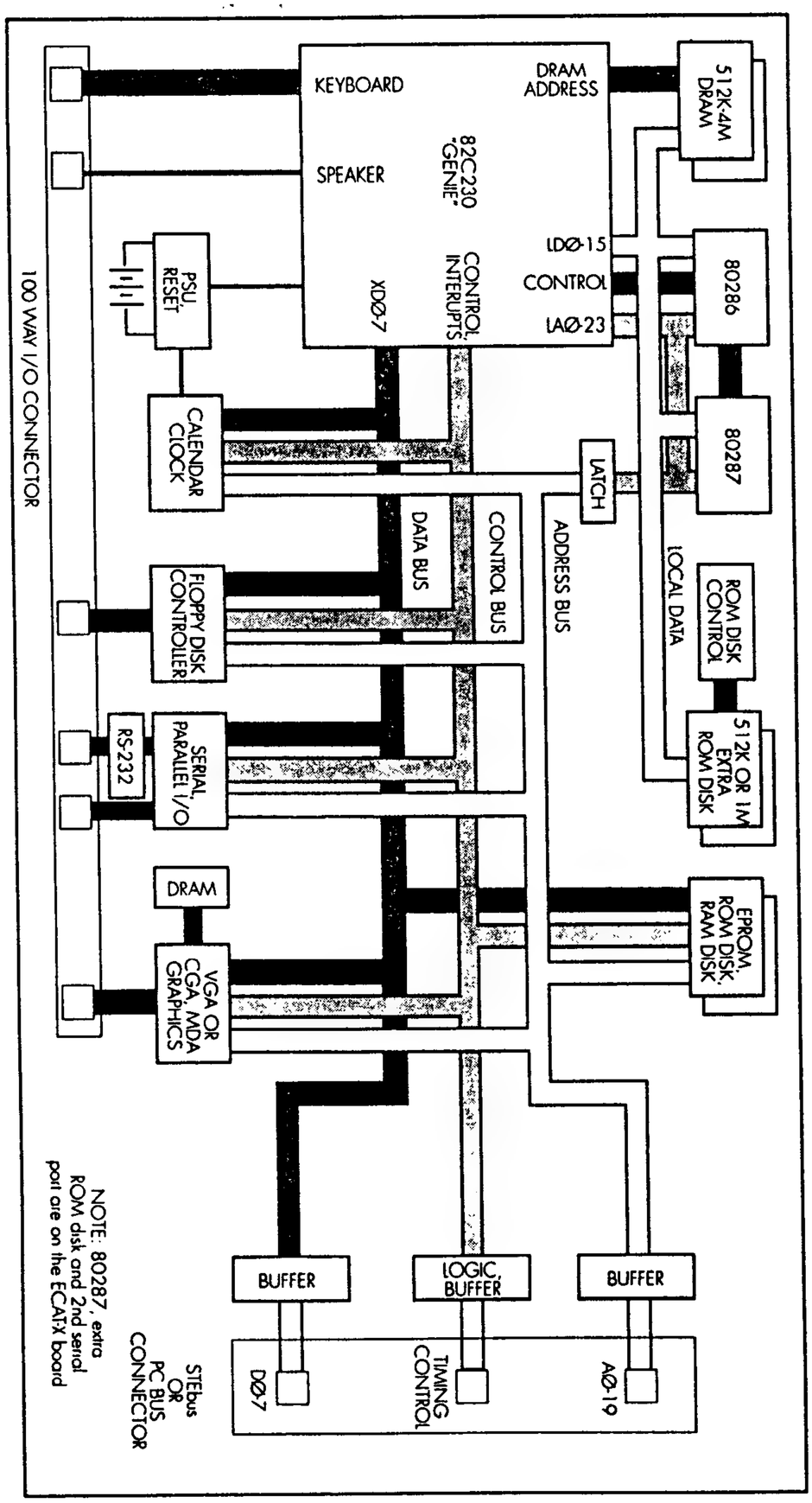


FIGURE 1 - ECAT BLOCK DIAGRAM

2 PROCESSOR, MEMORY AND GENIE CHIP

The ECAT features an 80286 processor, DRAM, and sockets for EPROMs. The standard ECAT (part number ECAT01) features 512k bytes of DRAM and a 64k byte EPROM for the BIOS, but address decoding is very flexible and a large number of memory configurations are possible.

2.1 PROCESSOR

The ECAT uses an 80286 processor running at 12.5MHz or 16MHz. The processor is usually an NMOS 80L286 from AMD, although fully CMOS 80C286 chips from Harris Semiconductor can also be used. The all CMOS chip reduces power consumption by about 250mA, to a mere 350mA, and of course runs cooler than the NMOS part.

The 12.5MHz ECAT scores 14.3 in the commonly used Norton Utilities SI test for processor speed. Other (perhaps more reliable) speed tests suggest that the ECAT runs 7.7 times faster than the original IBM PC.

2.2 GENIE CHIP

The ECAT computer is centred around the Genie chip from Chips and Technologies. This is a complex ASIC which provides a number of timing, control, address decoding functions and which includes a number of PC/AT compatible I/O peripheral circuits.

These peripherals are:

8237 compatible DMA control unit	(3 channels)
8254 compatible timer control unit	(3 channels)
8259 compatible interrupt control unit	(8 interrupts)
PS/2 Model 30 compatible keyboard port	

The other functions provided by the Genie are:

Clock generators for 80286, 80287 and timers.
Memory controller with on-board EMS registers.
Bus interfaces and conversion logic.
80287 support logic.
Peripheral I/O address decoding.

The majority of the peripheral functions are the same on all IBM compatible computers - the PC, XT, AT and PS/2. This includes the timers, interrupt controller and DMA controller. Thus software which accesses the IBM PC/AT peripherals will have the same effect when running on the ECAT, giving rise to a high degree of PC-compatibility, at

MS-DOS, BIOS and register level.

Some of the functions in the Genie chip are PS/2 Model 30 compatible rather than AT compatible. This includes the keyboard encoder and support logic for NMIs and the calendar clock. Since application software rarely access these resources except through BIOS calls the user is very unlikely to be aware of differences in these areas (the IBM PS/2 Model 30 is after all "PC compatible").

The Genie chip also includes a number of registers which have been introduced by Chips and Technologies. These control timing on the expansion bus, shadow RAM, DRAM configuration, EMS control and so forth. These are initialised by the BIOS and will not normally need to be accessed by the user.

2.3 DRAM

The main memory of the ECAT consists of Dynamic RAM (DRAM) chips. The chips used are 256k x 4 or 1M x 4 devices, which gives rise to four possible main memory options:

1)	512k bytes	(using 4 256k x 4 chips)
2)	1M byte	(using 8 256k x 4 chips)
3)	2M bytes	(using 4 1M x 4 chips)
4)	4M bytes	(using 8 1M x 4 chips)

The standard configuration of the ECAT (ECAT01) has 512k bytes of DRAM. The other two configurations can be ordered as factory-fitted options.

The DRAM is accessed using one wait state on the 16MHz board and zero wait states on the 12.5MHz version. (Early versions of the BIOS insert one wait state for the 12.5MHz version).

Note that only the first 640k bytes are usually directly accessible, conforming to the PC/AT memory map. If it is necessary to access more than 640k bytes within the 1M byte address space used by MS-DOS this can be achieved with a non-standard address decoder PAL.

Memory beyond the 640k byte limit can be accessed as bank switched memory (Expanded Memory) using the EMS memory mapping circuitry provided by the Genie chip. This memory is accessed as follows:

Between one and four blocks of 16k bytes each can be defined in the first 1M address space of the 80286 processor. These blocks are either between addresses D0000H-DFFFFH or E0000H-EFFFFH. These 16k byte blocks act as windows into the DRAM memory. By programming I/O mapped registers in the Genie chip each 16k byte block can be mapped onto any 16k block anywhere in the DRAM.

This mechanism is used by EMS software to access memory in excess of the 640k limit imposed by MS-DOS. EMS stands for Expanded Memory System and is a standard jointly proposed by Lotus, Intel and Microsoft (LIM). To use expanded memory the application software does not write directly to the mapping hardware, but interfaces to EMS driver software. At the time of writing an EMS driver does not exist for the ECAT but this is expected to change, so ask your dealer for details.

DSP Design are producing a driver to configure the extra expanded memory as a RAM disk.

2.4 BIOS EPROM - IC12

When shipped from the factory, a 64k byte EPROM containing the BIOS (Basic Input Output System) is fitted in the IC12 socket. This EPROM contains all of the machine-dependent software required in an MS-DOS computer.

Users who want a ROM-disk system can combine the BIOS and a ROM disk in a single EPROM, fitted in the IC12 socket. This ROM disk would often contain the MS-DOS operating system as well as the user's application program. ROM disks are described in sections 4.4 and 8.3.

IC12 is able to accept a variety of EPROM sizes - 32k, 64k, 128k and 512k bytes. The address decoder PAL and the E3 jumper area need to be adjusted accordingly.

The code in the BIOS is copyright American Megatrends Inc and DSP Design Ltd. The EPROM may not be copied.

The BIOS EPROM is an eight bit device which resides on the eight bit internal data bus. The Genie chip converts a 16-bit 80286 access to two eight bit accesses to the BIOS EPROM. The EPROM is accessed with several wait states. Systems with 1Mbyte or more DRAM can use "shadow RAM" in place of the EPROM. In this scheme the contents of the EPROM are copied to DRAM at the same addresses. The EPROM is then disabled and the BIOS is executed from the 16-bit wide DRAM with zero or one wait state.

At the time of writing the shadow RAM operation is not implemented but it may be at a later date. Ask your dealer for details.

2.5 OPTIONS FOR THE SECOND MEMORY SOCKET - IC11

In many applications the IC11 socket will remain unused. Alternatively, it can be populated with RAM or EPROM.

The IC11 socket may be fitted with one of several sizes of EPROM, which would usually be used as a ROM-disk. The ROM-disk can be used instead of, or as well as, floppy disk or hard disk drives, for storing program and data files. ROM disks are described in section 4.4.

Alternatively, IC11 can be a 32k or 128k byte static RAM chip. The RAM chip is mapped into the lowest 1M byte address space of the 80286 processor, so can be used as a general purpose data storage area, or it can be configured as a RAM disk.

This RAM can be made non-volatile with the addition of a battery back up socket (a "Smart Socket"). The smart socket is an IC socket which contains a small lithium battery and a circuit which switches the battery to the RAM's power supply pin when the main +5V power fails. The socket also disables the CE- pin, preventing data corruption. The part used is a Dallas Semiconductor DS1213D, which has the DSP Design part number BAT32D.

2.6 OTHER MEMORY OPTIONS, AND E3 JUMPER POSITIONS

The address decoder on the standard version of the ECAT (ECAT01) allows only for the 64k byte BIOS EPROM in IC12 and a 128k byte RAM or ROM disk in IC11. The hardware, however, has been designed to allow other devices to be fitted in IC11 and IC12, and these are described in Appendix E.

The jumpers at the E3 jumper area (below IC12) are set depending on the devices in IC11 and IC12. The standard version of the ECAT (the ECAT01) is shipped from the factory with the following links present at E3:

A2-A3
A4-A5
B2-B3
B4-B5
A8-A9
B7-B8

This set of jumper positions is for a 64k byte EPROM in IC12 and an SRAM in IC11.

2.7 MEMORY ADDRESS MAP

The address map on the ECAT is set in the PAL, IC1. A PAL is a programmable device which can be programmed in the factory to produce a variety of address maps. The standard version of the ECAT is shipped with a PAL labeled ECATADRX, which gives the memory map shown in Table 1. The address map will change depending on ROM disk and RAM disk requirements. Details of other memory maps are given in Appendix E.

Note that some early REV B boards have a PAL labeled ECATADR6 V1.0. This is equivalent to the ECATADRX.

In general, memory which is not present on the ECAT is mapped onto the STEbus.

Note that irrespective of the amount of DRAM present on the ECAT with the standard address decoding PAL (the ECATADRX PAL) the full 640k used by MS-DOS is mapped onto the ECAT and therefore accessing these addresses will not result in STEbus accesses. For users with 512k of DRAM fitted who would like to access STEbus memory in the range 512k-640k, special address decoding PALs are available. Please see Appendix E and contact your dealer.

ADDRESS	MEMORY DEVICE DECODED	ADDRESS
FFFFF ---		--- 1024k
	BIOS EPROM (IC12)	
F0000 ---		--- 960k
E0000 ---	ROM OR RAM DISK (IC11)	
D0000 ---		--- 832k
	STEbus	
C8000 ---		--- 800k
	VGA BIOS (ECAT-X)	
C0000 ---		--- 768k
B0000 ---	Video RAM	--- 704k
A0000 ---		--- 640k
	DRAM (if 1-4M of DRAM is fitted)	
80000 ---		--- 512k
40000 ---	DRAM	--- 256k
00000 ---		--- 0k

TABLE 1 - ECAT DEFAULT MEMORY ADDRESS MAP (ECATADRX PAL)

2.8 I/O ADDRESS MAP

The ECAT features a number of on-board I/O mapped resources, and supports access to the STEbus or PC bus I/O space as well.

All I/O mapped functions which are present on the IBM PS/2 Model 30 are present at the same I/O addresses on the ECAT. With the few exceptions previously noted these addresses are the same on the IBM PC, AT and PS/2 computers. The ECAT is therefore compatible at the machine code or register level with the IBM PC/AT.

On-board I/O devices include registers within the Genie chip as well as registers in the floppy disk controller, graphics controller, calendar/clock chip and the serial and parallel I/O chip. The on-board I/O address are listed in Tables 2 and 3. Table 2 shows the blocks of addresses which are

decoded by the address decoder PAL. In some cases these blocks are larger than required by the I/O port, but the address decoder has only 16 byte resolution. Table 3 lists the on-board addresses which are actually used, within the blocks defined in Table 2.

Those addresses which are not on-board are mapped onto the STEbus (or PC bus) I/O space. Users should however note carefully the comments on partial address decoding below.

ADDRESS	1ST ALIAS	2ND ALIAS	3RD ALIAS	I/O FUNCTION
000-0FF	400-4FF	800-8FF	C00-CFF	Reg.s in Genie
200-20F	600-60F	A00-A0F	E00-E0F	EMS Page Registers
2F0-2FF	6F0-6FF	AF0-AFF	EF0-EFF	COM2: Serial Port
350-35F	750-75F	B50-B5F	F50-F5F	Graphics Special Registers
370-37F	770-67F	B70-B7F	F70-F7F	Parallel Port
3B0-3DF	7B0-7DF	BB0-BDF	FB0-FDF	Graphics Reg.s
3F0-3F7	7F0-7F7	BF0-BF7	FF0-FF7	Floppy Disk Registers
3F8-3FF	7F8-7FF	BF8-BFF	FF8-FFF	COM1: Serial Port

TABLE 2 - ON-BOARD I/O DEVICES

ADDRESS	I/O FUNCTION
000-00F	DMA Controller in Genie
020-021	Interrupt unit in Genie
022	Internal Configuration Index Reg. - Genie
023	Internal Configuration Data Reg. - Genie
040-043	Timer Unit in Genie
060-06B	PS/2 I/O Reg.s - Keyboard etc in Genie
080-087	DMA Page Registers in Genie
0A0-0A1	Interrupt Control/Status Reg.s in Genie
0B0-0BF	Calendar/Clock Chip
0E0-0EF	Calendar/Clock Chip
208-209	EMS Page Registers
2F8-2FF	COM2: Serial Port
358-35F	72C81 Graphics Chip Special Registers
378-37F	Parallel Port
3B0-3BF	72C81 Graphics Chip Mono Registers
3D0-3DF	72C81 Graphics Chip Colour Registers
3F0-3F7	Floppy Disk Controller Registers
3F8-3FF	COM1: Serial Port

TABLE 3 - ON-BOARD I/O DEVICES

The 80286 chip has 64k byte I/O address range. In an IBM PC/AT, only the first 10 address lines are decoded, which gives a 1k byte I/O address space which is mirrored, or

aliased, 64 times through the 64k byte I/O space of the 80286. The STEbus Spec defines a 12 bit (4k byte) I/O address space.

The ECAT design maintains PC compatibility by decoding the first 10 address lines (A0-A9) for on-board I/O devices. I/O addresses which are not on the ECAT are mapped onto the STEbus. This allows PC compatibility while providing almost un-restricted use of the STEbus I/O space. The user should take care however to remember that only 10 address bits I/O are decoded onboard the ECAT.

As an example, the floppy disk controller is located at the 8 I/O locations starting at 3F0H, but because of the 10-bit decoding it is also accessible at (or "aliased" at) 7F0H, BF0H and FF0H (and higher addresses). It is therefore important not to try to access the STEbus I/O space at the base address or any of the three aliases. (This is particularly important when using some DSP Design I/O cards which are shipped configured for I/O addresses FF0H-FFFH.)

Although address bits A12-A15 are "don't care" bits as far as the STEbus is concerned during I/O cycles, users are advised to maintain these bits as zeros. In particular, A15 must always be a zero for I/O cycles, since when A15=1 STEbus vector fetch cycles will be performed (see section 5.4 for full details).

3 PERIPHERALS

The ECAT can connect to six peripherals - disk drive, CRT for video output, keyboard, speaker, serial port and parallel port. This section of the manual describes the features of each of these peripherals. Operation of the additional peripheral functions of the ECAT-X board (VGA graphics, second serial port, maths co-processor and ROM disk) are described in section 7.

3.1 FLOPPY DISK DRIVE

The ECAT can support one or two floppy disk drives. These can be 3.5" or 5.25" drives. Four PC-compatible formats are supported: 360k and 1.2M byte 5.25" drives and 720k and 1.44M bytes 3.5" drives. The standard BIOS is configured to operate with 3.5" and 360k byte 5.25" floppy disk drives. If you want to use 1.2M byte 5.25" disks a different BIOS is required - contact your dealer for details.

A SCSI hard disk can be supported with the addition of a second STEbus card - see section 4.7.

Connection is made to the disk drives through 34 signals on one of the 50-way ribbon cables. If you order your ECAT with a terminated cable assembly (part number ECAT-BP), then a 34 way connector suitable for a 3.5" floppy drive will already be fitted to this cable, and power can be delivered to the disk drive through a 4-way power supply connector also mounted on the cable (this supplies +5V only - drives with +12V requirements cannot use this connector).

Appendix F gives the pin assignments for the 34-way floppy disk drive cable. The floppy disk controller uses interrupt level IRQ6 and DMA channel 2. Further details of floppy disk operation is given in section 4.3.

3.2 VIDEO PORT

The ECAT supports a variety of video options for driving CRT displays.

- IBM compatible monochrome (MDA) - alphanumeric
- Hercules compatible monochrome - alphanumeric and graphics
- IBM colour graphics (CGA) - alphanumeric and graphics, with 40 character and 80 character modes
- Hi-Def (double scan) CGA - alphanumeric and graphics, with 40 character and 80 character modes

VGA and EGA graphics are available by adding the ECAT-X board to the ECAT (see section 7).

All modes are IBM compatible and run standard software. Table 4 summarizes the features of each of the modes:

MODE	TYPE	ALPHA FORMAT	CHAR CELL	SCREEN RESOLUTION	NUMBER OF COLOURS	DOT CLOCK (MHz)	HORIZ FREQ (KHz)	REFRESH FREQ (Hz)
MDA	Alpha	80x25	9x14	720x350	3	16.0	18.432	50
Hercules	Graphic	80x25	9x14	720x348	2	16.0	18.432	50
CGA	Alpha	40x25	8x8	320x200	16	14.3	13.750	60
CGA	Alpha	80x25	8x8	640x200	16	14.3	15.750	60
CGA	Graphic	40x25	8x8	320x200	4	14.3	15.750	60
CGA	Graphic	80x25	8x8	640x200	2	14.3	15.750	60
Hi-Def	Alpha	40x25	8x6	320x400	16	20.0	25.000	57
Hi-Def	Alpha	80x25	8x16	640x400	16	20.0	25.000	57
Hi-Def	Graphic	40x25	8x16	320x400	4	20.0	25.000	57
Hi-Def	Graphic	80x25	8x16	640x400	2	20.0	25.000	57

TABLE 4 - AVAILABLE VIDEO MODES

The MDA, Hercules and CGA modes will be familiar to PC users. The Hi-Def, or double scan modes are variations of the CGA modes. In Hi-Def mode each CGA line is drawn twice, giving a much better looking display.

As can be seen from Table 4, the monochrome modes require a 16MHz dot clock, the CGA modes a 14.3MHz clock and the Hi-Def modes a 20MHz clock. These clocks are selected at the jumper area marked E8. The video mode must be selected by selectively installing two 1k ohm resistors on the ECAT board. Table 5 shows the jumper setting and resistors required.

DISPLAY MODE	E8 LINK	RESISTORS
Monochrome	link 4-5	Fit R7 only
CGA	link 3-4	Fit neither
Hi-Def	link 1-2	Fit R6 only
Disable ECAT graphics	link 4-5	Fit R6 and R7

(Note: Pin 1 on E8 is towards the top of the ECAT)

TABLE 5 - CONFIGURING GRAPHICS MODE

The Hi-Def modes require the addition of a 20.0MHz crystal and a capacitor. This can be done by the user, or by DSP Design. (Contact your dealer if you require Hi-Def crystals fitted at the factory.) To fit the components for the Hi-Def mode, follow these instructions:

1 remove the wire link in the C12 position

2 install a 33pF ceramic capacitor in place of the wire link
3 install a 20.0MHz crystal in the X1 position

Once a video mode has been selected with the resistors and jumpers the MS-DOS and application software will do the rest, filling the screen with text or graphics according to the selected mode.

Users who require EGA or VGA graphics should fit the ECAT-X card (see section 7). The ECAT standard graphics should be disabled, or preferably a partially depopulated version of the ECAT should be used. This is the ECAT03G. A two board set is available, called the ECAT03GX.

A PC-compatible 9 pin female D-type connector for video monitors is mounted on the aluminium panel which forms part of the ECAT terminated cable assembly. This has the part number ECAT-BP, or ECAT-BPX if the ECAT-X is used.

The ECAT can be adapted to drive electro-luminescent and plasma displays. In addition a card which will support LCD graphics is also being developed. (An LCD version of the ECPC is aready in production). Contact your distributor for further information.

3.3 KEYBOARD

The ECAT requires an IBM AT keyboard which support Scan Code set 1. Note that some AT keyboards support only Scan Code Set 2 - these will not work with the ECAT. Many keyboards operate in both modes as well as IBM PC mode, and have a switch to select PC/XT or AT operation. DSP Design can supply a suitable keyboard.

In many applications the familiar desktop keyboard is inappropriate. A variety of of industrial keyboards and keypads are available - contact your dealer or DSP Design for details.

A PC-compatible 5 pin DIN connector for the keyboard is mounted on the aluminium panel which forms part of the ECAT terminated cable assembly.

Users should avoid plugging in the keyboard when the ECAT is powered on.

3.4 SPEAKER

A PC-compatible loudspeaker port is implemented on the ECAT. This allows for production of tones, tunes, keyboard clicks etc. PC software which generates sound will therefore operate as expected with the ECAT.

The ECAT terminated cable assembly (ECAT-BP) incorporates a small loudspeaker, which is mounted on the rear of the aluminium panel.

3.5 SERIAL PORT

The ECAT features an RS-232 serial port which is accessed as COM1:. A second serial port (COM2:) is available on the ECAT-X add-on board.

The serial port is fully hardware and software compatible with the IBM PC/AT serial port and all PC communications software packages will work with the serial port. Connection is made to the serial port via a 9 way male D-type connector mounted on the ECAT-BP cable assembly front panel. This connector is compatible with pin assignments used on IBM AT computers.

The serial port provides the full complement of RS-232 signals: Transmit Data, Request To Send (RTS) and Data Terminal Ready (DTR) are outputs from the ECAT, and Receive Data, Data Carrier Detect (DCD), Data Set Ready (DSR), Clear to Send (CTS) and Ring Indicator (RI) are the inputs to the ECAT.

Following a reset of the ECAT the serial port is initialized as follows:

baud rate :	2400	stop bits :	two
data bits :	8	parity :	none

These parameters can be changed by the MS-DOS MODE command.

The KERMIT public domain file transfer and terminal emulator package can be used with the ECAT. It is supplied on the ECAT utilities disk, part number ECAT-UTIL.

The COM1: serial port uses interrupt level IRQ4 to interrupt the processor. It should be noted that the BIOS does not make use of serial port interrupts, but that most comms software packages enable the interrupt and make use of it to increase the speed of serial data transfer.

Due to a lack of pins on the 100 way I/O connector, and also to ensure compatibility with the ECPC computer, the COM2: signals are not brought out on the 100 way connector. The signals are taken to a connector on the the ECAT-X board.

3.6 CENTRONICS PRINTER PORT

The ECAT implements a full-function Centronics compatible printer port. This port is the MS-DOS PRN: device.

The Centronics port features an 8-bit data port and the full compliment of control signals - four output signals and five input signals.

The I/O signals on the printer port can be treated as general purpose digital input and output signals, and as such can be used for other applications (such as driving a small LCD display, for example). DSP Design may be able to help with information on driving the parallel port for non-standard applications.

The data port is normally used as an output port for driving a printer. It can be used as an input port however. Bit 7 of I/O address 65H in the Genie chip (The Planar Control Register) controls the direction of the parallel I/O port. A 1 sets the port to be an output and a 0 sets it to be an input. Users who wish to change this bit should ensure that no other bits are changed (the port is read/write so this can easily be done).

The Centronics port is accessed via a PC-compatible 25 way female D-type connector which is mounted on the aluminium panel which forms part of the ECAT terminated cable assembly (the ECAT-BP).

The parallel port uses interrupt IRQ7 to interrupt the processor.

3.7 CALENDAR CLOCK CHIP

Calendar/clock functions are provided by a National Semiconductor MM51867 chip. This chip provides time of day functions as well as calendar functions. An alarm facility is also provided - this allows an interrupt to be generated when a particular time is reached.

The calendar/clock chip should be accessed through the MS-DOS calls (interrupt 1AH).

A battery provides power to maintain the clock when the main power is not present. Because of board space limitations the battery is of limited capacity. It is estimated that it should be sufficient for the clock to operate for about 2 years in the absence of the +5V power supply. For this reason the jumper E2 is provided which can be used to disconnect the battery in order to extend the battery life. The battery should be disconnected while the ECAT is in

storage.

In REV B versions of the ECAT the battery is a lithium battery, which is not rechargeable. In Rev C versions a Rechargeable Nicad battery is used. The Nicad is trickle charged from the +5V supply when the ECAT is powered on.

At the time of writing the TIME and DATE commands do not automatically update the calendar/clock chip after it has been powered down. DSP Design provides a program called SETCLOCK which can be run to initialise the calendar clock after reconnecting the E2 jumper. After this program is run the TIME and DATE commands can be used to set the time and date. This program is available on the ECAT-UTIL utility disk.

PCB revisions REV C and later have a variable capacitor which is used to adjust the frequency of the calendar/clock crystal oscillator.

4 DISK DRIVE OPTIONS

The ECAT will support a number of types of disk drives, both mechanical and solid state. These are: floppy disks, SCSI hard disks, ROM disks and RAM disks. ROM disks and RAM disks disks are mentioned elsewhere, but the detailed information is brought together in this section for convenience.

4.1 COMBINATIONS OF DISK DRIVES

The ECAT will support the following disk drives:

zero, one or two floppy disks
zero to four ROM disks
zero, one (or more) RAM disks
One SCSI disk (more may be supported later)

Any combination of the above drives is possible, except that ROM disks and SCSI disks cannot currently both be present simultaneously. Ask your dealer is you require this particular combination.

4.2 DRIVE LETTER ALLOCATION AND BOOT SEQUENCE

There are a number of rules concerning the allocation of drive letters and the sequence in which drives are examined for a bootable MS-DOS. The rules are listed below:

In systems without ROM disks, following reset the BIOS searches for a disk containing MS-DOS in the following sequence:

1 The first floppy disk drive (the second floppy is not checked).
2 The SCSI drive.

In systems without ROM disks the two floppies are always A: and B:. The SCSI drive is C: if it is fitted. Any RAM disks are allocated the next available drive letter(s) - eg a RAM disk would be C: in systems without a SCSI disk and D: in systems with SCSI disks.

In systems with ROM disks the drive from which MS-DOS boots can be a floppy or a ROM disk and this boot drive is always the A: device. However it is possible for the user to define the allocation of drive letters in drive allocation tables which are blown into the ROM disk EPROMs. These tables are examined following reset and drive letters are allocated to the floppy disk drives and ROM disks. Two tables are used - one is used under normal circumstances and the other is used if a particular key is pressed within a few seconds of reset.
The reason for having two tables is primarily to allow a

floppy disk to be used from time to time to boot a system with MS-DOS in EPROM. This is explained below.

A typical ROM disk system will have one or two ROM disks and one floppy disk drive. The default drive allocation table would typically configure the two ROM disks as A: and B:, and the floppy would be C:. MS-DOS will be loaded from the A: ROM disk and it is possible to power up with a floppy disk installed in the C: floppy disk drive.

The alternative drive allocation table would typically configure the floppy as A: and the two ROM disks as B: and C:. Following reset a message on the screen invites the user to type a key, and if this key is pressed within a few seconds, the alternative drive allocation table is selected and the floppy disk is used for booting MS-DOS. (The key to press can be defined in the drive allocation tables themselves).

The two different drive allocation tables therefore allow the floppy disk drive to be either ignored during the boot process, or to be used to load MS-DOS.

It is even possible to design the drive allocation tables so that a particular ROM disk is allocated two different drive letters - A: and C: for instance. This allows the tables to be designed to avoid problems that might arise if drive letters changed when booting from a floppy.

A program called MKECROM is used to build a ROM disk driver with the customised sets of drive allocations. Section 8.3 gives more information on programming ROM disks.

In systems with ROM disks SCSI drives cannot be fitted. RAM disks are allocated the next available drive letters following the floppy disks and ROM disks.

4.3 FLOPPY DISK DRIVES

One or two floppy disk drives are supported by the ECAT. These can be either 3.5" or 5.25" drives, although the standard BIOS supports only 3.5" drives and 360k byte 5.25" drives. Users who want to use 1.2M byte 5.25" drives should contact their dealer.

Both 720k and 1.44M byte 3.5" formats are supported. Many 3.5" floppy disk drives, including the two listed below, identify a high density (1.44M byte) floppy disk by the presence of a hole in the disk case on the opposite side from the write protect hole. Be sure to use this type of disk if you are using the 1.44M byte format.

Connection is made to the disk drives through 34 signals on one of the 50-way ribbon cables. If you order your ECAT

with a terminated cable assembly (the ECAT-BP) then a 34 way connector suitable for a 3.5" floppy drive will already be fitted to this cable, and power can be delivered to the disk drive through a 4-way power supply connector also mounted on the cable (this supplies +5V only - drives with +12V requirements cannot use this connector).

Appendix F gives the pin assignments for the 34-way floppy disk drive cable. Unfortunately, although this pin assignment is "standard" some older drives use different pin assignments, so users should ensure that they are using an appropriate disk drive, and that the drive is jumpered correctly.

In particular, users should check on the functions of the following pins on their disk drive.

Pin 1 : Should be GND (0V) or not connected.

Pin 2 : Should be a "High Density" input, or not connected. If the pin is a High Density input, it must be configured such that a logic 0 on this pin represents High Density operation. The preferred mode of operation is for this pin to be not connected.

Pins 4, 6 : These are not connected on the ECAT.

Pin 14 : This pin should be not connected on the disk drive (it is connected to Motor On 1 on the ECAT).

Pin 16 : This pin should be "Motor On" input on the disk drive.

Pin 34 : This pin should be a "Disk Change" output from the disk drive (some drives use pin 34 as a Ready output).

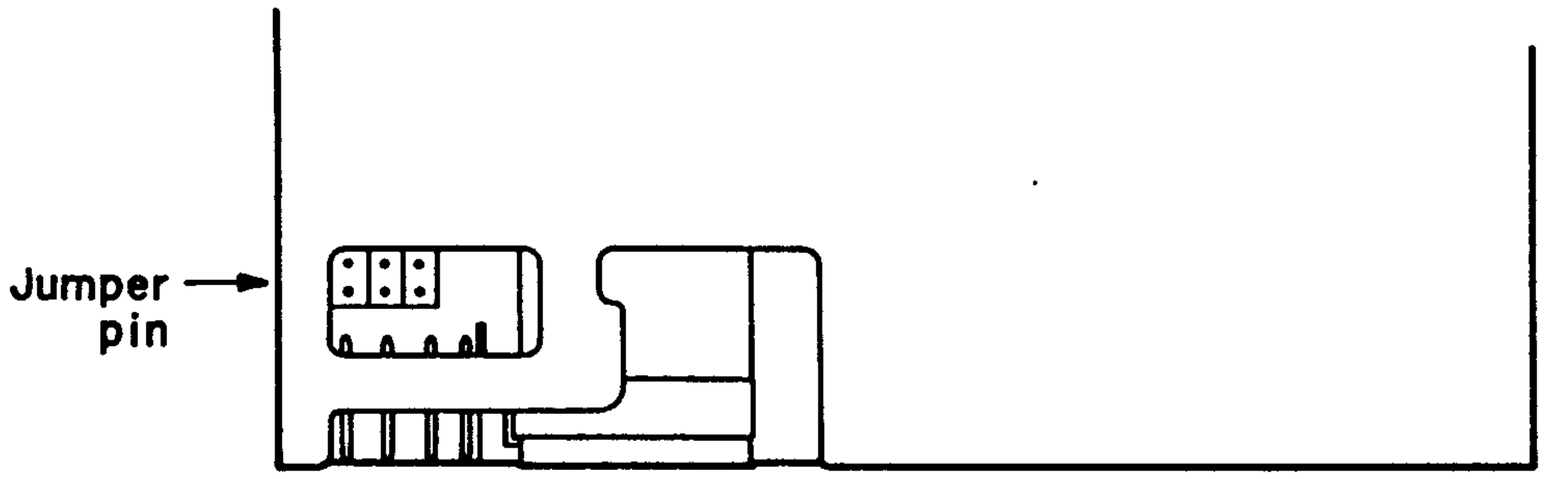
DSP Design can recommend two 3.5" floppy disk drives as being suitable for use with the ECAT (there are obviously others which are suitable; these two have been used extensively at DSP Design and found satisfactory).

1 Teac FD-235HF

Install jumpers of the jumper header at the D0 and OP positions. No jumpers should be present on the HHO, LHI, HHI or D1 positions.

2 Citizen OSDA-08C

Switch DSSW1 should be set to position "0" The jumper immediately above the power supply connector should be set as shown in the diagram below. Option C should be selected.



	No 2.		Jumper Pin Position
A	Input	Low=2MB, High=IMB	
B	Input	Low=IMB, High=2MB	
C	Open	Mode is changed by internal sensor	

FIGURE 2 - CONNECTION OF JUMPERS ON CITIZEN DISK DRIVES

The standard version of the BIOS supports two 3.5" floppy disk drives, or 360k byte 5.25" drives. The 3.5" disks can be either 720k or 1.44M bytes. If you need 1.2M byte 5.25" drives, contact your dealer. The BIOS will automatically adapt to the type of floppy disk used. If either of the two 3.5" drives mentioned above are used, and you want to make use of 1.44M byte format floppies, then "high density" floppy disks must be used. These floppies have a hole (opposite the write protect hole) which allows the drive to identify the disk as a high density disk and switch mode appropriately.

Floppies can be formatted with the standard MS-DOS FORMAT

command. If formatting 720k byte 3.5" floppies be sure to use the /N:9 option (see your MS-DOS manual for details).

If two floppy disk drives are to be used with an ECAT then both drives are connected on the same cable, with the second drive configured as unit 1 (the first drive being unit 0). Disk drives will have a switch or a jumper allowing them to be configured as drive 0 or 1. Drive 0 will be assigned to the lower drive letter (eg A:) and drive 1 to the next letter (eg B:).

The floppy disk cable must be modified to accommodate the second drive, as follows.

The 34 way connector for the first floppy disk drive is crimped to the cable as normal, a few centimeters from the end of the cable. Between this connector and the end of the cable five wires from the cable are split off and twisted through 180 degrees. The 34 conductors of the cable are then placed in the second 34 way connector and the connector crimped. This half twist routes drive select and motor on signals to the correct pins on the second drive.

The five conductors which are twisted are pins 13-17 of the 34 way cable (21-25 of the 50 way cable). This cable assembly results in the connector closest the ECAT being used for the first floppy disk (eg drive A:) and the connector furthest from the ECAT being used for the second floppy disk (eg drive B:).

If a second drive is used then a second power supply connector can be fitted to the previously unused 8 wires of the ribbon cable. Reference to the pin assignments of the cable in Appendix F will allow you to fit this connector.

4.4 ROM DISK OPTIONS

A key feature of the ECAT is the ability to operate without mechanical disk drives (either floppy disks or hard disks). To do this the user may substitute EPROMs which appear to the ECAT software as disk drives. These EPROMs are termed ROM disks. As well as being more robust than mechanical drives, ROM disks are also very much faster.

ROM disks, since they are implemented with EPROM chips, are inherently read-only devices. However the EPROM chips can be replaced by RAM chips, and a RAM disk created. The RAM disk is a read-write device, and if the RAM is supported by a battery back-up circuit the RAM disk will be non-volatile (that is, its data will be retained when the ECAT is switched off). Section 4.5 describes RAM disks.

A ROM disk is created by taking an exact image of floppy disk and transfering the data into an EPROM with a PROM

programmer. On the ECAT utilities disk DSP Design provides software to assist with the development of ROM disks. The process is described in detail in section 8.3. The remainder of this section gives an overview of the options available.

A number of ROM disk options exist for ECAT users and DSP Design are constantly adding new options. Amongst those available are:

1 Combining the BIOS, MS-DOS and user files in a single ROM disk in the IC12 socket (using a 256k byte EPROM).

2 A 128k or 256k byte ROM disk in the IC11 socket.

3 256k, 512k or 1M byte ROM disk on the ECAT-X card.

4 Larger ROM and RAM disks implemented on STEbus memory cards.

For small sized ROM disk requirements the first option above is recommended. The BIOS can be combined with the MS-DOS operating system and the user's application code and blown into a single 256k byte EPROM in the IC12 site. About 73k is available for the user's program and data files. This option allows the ECAT to boot MS-DOS from EPROM following a reset. An AUTOEXEC.BAT file transfers control to the user's application program as soon as MS-DOS has been loaded.

The second ROM disk option allows a ROM disk to be fitted in the IC11 socket. The IC11 ROM disk can be used either with or without the combined BIOS and MS-DOS ROM disk in the IC12 socket.

The EPROM in the IC11 socket can be one of several sizes. The most practical sizes are 128k and 256k byte chips, and the Intel 27011 bank switched 128k byte chip. The 27011 chip is a 128k byte device arranged as eight 16k byte pages. This allows the 128k bytes to occupy only 32k bytes of the ECAT's address space (32k byte blocks is the smallest block which can be decoded by the ECAT address decoder).

The third option is to add large ROM disks on the ECAT-X card. The ECAT-X add-on board includes support for ROM disks making use of the EMS memory mapping functions of the Genie chip. This mechanism allows the ECAT-X ROM disk to be bank switched into a small window in the 1Mbyte address space of MS-DOS, and since this window can be enabled and disabled dynamically the effect is that the ROM disk occupies none of the valuable 1M byte memory space.

The forth option allows users to add extra STEbus boards to their system. Memory boards of 256k byte and 1M byte capacity are available. Larger memory boards may become available soon. If the 27011 chips are used on the SM256 STEbus memory cards a 1Mbyte ROM disk will occupy only 128k

bytes of the ECAT's 1Mbyte memory space.

Any or all of these four alternatives can be used, with or without a RAM disk. Users needs to consider their program size and hence heir disk requirements, and plan their memory maps accordingly. Different address decoder PALs will be required by different address maps.

The fundamental constraint on ROM and RAM disk options is the 1Mbyte memory limit imposed by MS-DOS and the 80286 processor (in protected mode). Of this 1Mbyte some must be taken up by DRAM and almost all systems require 64k to be allocated to video memory (EGA and VGA systems need 128k for video memory and 32k for the EGA BIOS ROM). The remaining memory space can be used by ROM and RAM disks, both on the ECAT and on the STEbus. Clearly a large ROM disk means less DRAM is available, and vice versa. ECAT-X ROM disks occupy none of the 1Mbyte address space.

A large number of workable ROM and RAM disk configurations have been implemented by our customers, and consequently a large number of address decoders have been produced. Appendix E lists many of these address maps and users are advised to look at this appendix since a suitable address map probably already exists.

The steps towards implementing a ROM disk are thus as follows:

1 Determine required ROM and RAM disk sizes.
2 Use Appendix E to select an appropriate memory map.
3 Use the instructions in section 8.3 and the software supplied on the ECAT utilities disk to program the ROM disk.

4.5 RAM DISK OPTIONS

The ECAT can support a number of RAM disk options.

The first option is the RAM disk driver which is provided with MS-DOS. This turns part of the main DRAM of the ECAT into a RAM disk. This RAM disk is of course volatile - that is it looses its data when the ECAT is reset.

The second option for users who want to use DRAM beyond the 1Mbyte limit is to use DSP Design's Expanded Memory RAM disk driver.

The third set of options provide non-volatile RAM disks and involve using a RAM disk driver provided by DSP Design. This driver assumes that the user has provided battery-backed Static RAM somewhere in his system - either in the IC11 socket or on an STEbus memory card. The RAM disk driver converts this RAM into a RAM disk and allows the user to

store files in the RAM disk which will be retained while the computer is turned off.

The RAM disk driver will support a number of RAM disk types:

1 A 32k or 128k byte RAM chip installed in IC11 with a Dallas Smart Socket to provide battery back-up.

2 An SM256 STEbus memory card present on the STEbus. This card includes battery back-up circuitry.

3 The new SM1000 memory card which can provide up to 1M byte of battery backed RAM on the STEbus (this card is being designed at the time of writing).

The DSP Design RAM disk driver takes the form of a .SYS file which is loaded when MS-DOS is booted. The driver, called ECRAM.SYS, is placed on the boot disk and an entry is made in the CONFIG.SYS file to ensure that it is loaded following reset.

The RAM disk driver is available on the ECAT Utilities disk (part number ECAT-UTIL). Full documentation comes with this disk. Further information on the RAM disk driver software is given in section 8.4.

4.6 EEPROM ROM DISKS

The ECAT-X card has been designed to accept Flash Electrically Erasable PROMs, or EEPROMs. These chips can be erased and programmed by software, and the data programmed into them is retained when the power is switched off. Flash EEPROMs require a high programming voltage, typically 12.5V, which must be provided by an external voltage source.

DSP Design plans to produce a ROM disk driver suitable for use with EEPROMs. Ask your dealer for details.

4.7 SCSI HARD DISK

The ECAT can be used with a SCSI hard disk. The SCSI disk is controlled by DSP Design's SF840-S disk controller card, which plugs into the STEbus. MS-DOS can be installed on the SCSI drive so that the operating system boots from the hard disk, just like a conventional IBM AT computer.

At the time of writing an additional BIOS EPROM, which plugs into the IC11 socket, is required to provide the driver for the SCSI drive. The SCSI driver may soon be be incorporated into the main BIOS EPROM.

DSP Design recommends the Seagate ST138N SCSI disk drives and can supply these drives. The BIOS may not support other

drives, since there are differences in the way the SCSI command set is implemented by different manuafacturers, so contact your dealer before buying other types.

The installation procedure for SCSI drives consists of the following steps:

1 Configure the ECAT for the driver EPROM.
2 Configure the SF840-S SCSI controller card.
3 Format the SCSI disk.

These steps are outlined in further detail below:

1 Configuring the ECAT

The EPROM containing the SCSI driver code is labelled ECATHD, and contains a device driver which is located in the EPROM search, following reset. The driver code is 2k bytes in size, and although it can be placed at any 2k byte boundary in the range A0000H - EF800H it is normal to locate the driver in 64k byte EPROM by itself in the IC11 socket at address E0000H, using the ECATADR7 address decoeder PAL.

Alternatively the code can be copied from the 64k byte ECATHD EPROM supplied by DSP Design and blown into a different EPROM (it could be combined with the main BIOS EPROM in a 128k byte EPROM so as to occupy just the IC12 socket).

Therefore to configure the ECAT the SCSI driver code should be incorporated in a suitable EPROM and installed in one of the ECAT memory sockets, and Appendix E should be used to select a suitable address decoder PAL and to set the E3 jumpers. Note that the memory area allocated by the address decoder PAL should match the size of the actual EPROM used, since problems will occur if the EPROM is aliased (eg by fitting a 64k byte EPROM into a 128k byte address space).

2 Configuring the SF840-S

The DSP SCSI driver is used with the SF840-S SCSI controller card. The SF840-S is set to I/O address 310H. The jumper settings on this card are:

E1: One jumper linking B-C.
E2: No jumpers fitted.
E3: B0-C0, A1-B1, A2-B2, A3-B3, B4-C4, B5-C5, A6-B6, A7-B7
E5: B0-C0, B1-C1, B2-C2, B3-C3, A4-B4, B5-C5, A6-B6, A7-B7

3 SCSI Drive Set-up

There are four phases to be performed as follows:

1 Set the SCSI Unit Number on the drive to 1. (There is a switch or jumpers on the drive to allow you to do this).

2 Low level format - this depends on the drive supplied and is not necessary for the ST138N recommended by DSP.

3 Boot up from the floppy drive and run FDISK (supplied on the MS-DOS master disks) to partition the drive. This is described in MS-DOS manuals.

4 Reboot from the floppy and run "FORMAT C: /S /V", this will format the drive ready for use and install the MS-DOS system files. This is described further in the MS-DOS manuals supplied with the MS-DOS system disks.

If the driver does not recognise the hard disk or the controller card the message "1701" will be displayed. If the disk is not located there will be a long wait before the system boots from floppy - the driver thinks that the drive has not yet run up to speed.

5 STEbus AND PC BUS INTERFACES, AND STAND-ALONE OPERATION

The ECAT will operate as a single board computer, or can use its STEbus interface to expand its capabilities, with the wide range of STEbus I/O cards. A version of the ECAT can drive PC bus cards rather than STEbus cards.

This section of the manual describes first the stand alone operation and then operation on the STEbus. At the end of each section relating to STEbus operation any differences between the STEbus and PC bus version are noted.

5.1 STAND-ALONE OPERATION

The ECAT will operate as a single board computer with the addition of the appropriate peripherals (keyboard, monitor etc) and a single +5V power supply. In stand-alone operation the ECAT need not be plugged into a bus.

The ECAT requires a +5V power supply, with +/- 10% tolerance. Power can be supplied in a number of ways.

One power supply option is to use the "Powerterm" product from DSP Design (part number PT-1). The Powerterm includes a voltage regulator circuit mounted on a small PCB which plugs into the ECAT STEbus connector (J1). Either regulated DC, unregulated DC or AC can be connected by screw terminals to power the ECAT.

Power can be supplied to the PC bus version of the ECAT through the PC bus connector, J1. The +5V should be applied to any or all of pins a0, b3 and b29. The 0V should be applied to any or all of pins b0, b1, b10 and b31.

The third power supply option is to provide the PC bus version of the ECAT with power through the 100 way J2 connector and ribbon cable. The +5V should be applied at any or all of pins 5-8 and 47-50 on the bottom 50 way ribbon cable. The 0V should be applied at any or all of pins 1-4 and 43-46 on the bottom cable. The user should consider the likely voltage drop along this ribbon cable and chose a cable length and number of pins used accordingly. (Too much voltage drop will cause the power supply monitor circuit to reset the ECAT).

The STEbus version of the ECAT should only be used in a stand alone manner if bus input pins are tied to a logic 1 signal. This is done automatically by the Powerterm. If tying these pins high is not possible then use the PC bus version of the ECAT for stand alone operation.

5.2 STEbus AND PC BUS DATA TRANSFER

The ECAT performs STEbus memory read and write cycles, I/O read and write cycles, and vector fetch cycles.

If the address decoding circuit detects a memory or I/O access to an address which is not on-board the ECAT then an STEbus access will be initiated. Until such a cycle begins the ECAT does not drive any of the STEbus data transfer lines (the address, data and CM bus, and the data and address strobes).

An STEbus access is performed with the STEbus address being the same as the 80286 address. Sixteen bit data transfers are translated by the Genie chip into two consecutive 8-bit transfers.

The STEbus cycle begins with the address bus, CM lines and (for write cycles) the data bus being driven to the appropriate values. Then the ADRSTB* and DATSTB* signals are asserted. The addressed STEbus slave card responds by asserting the DATACK* handshake signal. The ECAT removes ADRSTB* and DATSTB*, and then stops driving the address, data and CM buses.

If no slave card responds with DATACK*, the ECAT will terminate the cycle by asserting the TFRERR* signal. This is done by a bus timeout circuit on the ECAT. In the standard configuration the TFRERR* signal is asserted approximately 6us after DATSTB* is asserted. This time-out period can be changed by changing the value of the capacitor C11 which is located between IC2 and the STEbus.

Table 6 lists values for C11. These times are only approximate (say +/- 30%), and the timeout periods will be less for the 16MHz version of the ECAT. Timeout periods longer than the standard 6us may be required by I/O cards (such as A/D convertors and disk controllers) which take longer than average to supply valid data. Check the manual of the slave card to determine the access times.

Timeout Period (us)	Capacitor Value
1.5	100pF
3	220pF
6	390pF
15	1nF
30	2.2nF
150	10nF

TABLE 6 - TIMEOUT CAPACITOR VALUES

PC bus transfers use the familiar PC bus timing signals: MEMR-, MEMW-, IORD-, IOWR-, ALE, IOCHRDY, CLK etc. Unlike the STEbus cycles are extended by slow peripherals by pulling the IOCHRDY signal low. Consequently there is no need for the timeout circuit, which is not implemented. Unlike the STEbus address, data and control signals, the PC bus signals are driven continuously.

5.3 CLOCK AND RESET SIGNALS

The ECAT can provide the STEbus SYSCLK signal. This is a 16MHz signal which is normally supplied by the processor card. If SYSCLK is not required, remove the jumper at E6.

The ECAT can reset, or be reset by, the STEbus. See section 6 for details.

In the PC bus version two clocks are provided: the bus clock (CLK) and an asynchronous oscillator (OSC). The OSC signal is a clock running at 14.3181MHz. The PC bus clock runs at the same speed as the processor clock (12.5MHz or 16MHz). If this is too fast a change can be made in the BIOS ROM. Ask for information if this is required.

The PC bus version drives the PC bus RESET signal. The ECAT cannot be reset by the PC bus RESET signal.

5.4 INTERRUPTS

The STEbus can interrupt the ECAT using some of the ATNRQn* signals. Table 7 lists the ATNRQn* pins and the corresponding IBM PC/AT interrupt and the interrupt vector number.

ATNRQn*	Int. Vector Number (Dec)	Equivalent IBM PC/AT Signal
0	2	I/OCHCK- (Non Maskable Interrupt
1	10	IRQ2
2	11	IRQ3 *
3	-	DACK1-
4	13	IRQ5
5	-	DRQ1
6	-	DRQ3
7	-	DACK3- or T/C

* see text

TABLE 7 - USE OF ATNRQn* SIGNALS

Interrupt IRQ3 can optionally be used by software driving the COM2: serial port, although it is not used by MS-DOS or the BIOS. If IRQ3 is to be used by the COM2: software then jumper E5 should be removed. If IRQ3 is to be driven by ATNRQ2* the jumper should be left in place.

Note that the DMA Request pins can be used as extra "low performance" interrupts, by programming the DMA channels to transfer a single byte, and polling the DMA transfer complete bit periodically.

The ECAT can perform STEbus vector fetch cycles. These are bus cycles which read an 8-bit value known as an interrupt vector from an STEbus slave card which is asserting an interrupt. This vector can be used to identify the source of the interrupt and so greatly speed up interrupt service routines.

On receipt of an STEbus interrupt the 80286 jumps to the interrupt service routine pointed to by the 80286's interrupt vector table (see Table 7 above). Once in this interrupt service routine the user can, optionally, perform a vector fetch cycle to read an interrupt vector from the interrupting slave card. The vector is read into the AL register by executing an 80286 input instruction (IN AL,DX) from an address with A15=1. Table 8 gives a range of suitable addresses.

In most microprocessor designs interrupt vectors are read during the processor's interrupt acknowledge cycle and used to directly "vector" the processor to an appropriate interrupt service routine. Hardware details of the 80286 and STEbus mean that this is not possible with the ECAT, so the indirect method of reading the interrupt vector by performing an input instruction must be used.

ATNRQn*	I/O ADDRESS TO READ VECTOR FROM
0	8300H
1	8301H
2	8302H
3	8303H
4	8304H
5	8305H
6	8306H
7	8307H

TABLE 8 - VECTOR FETCH ADDRESSES

The PC bus does not support vectored interrupts. In the case of the PC bus the following interrupt signals are connected directly from the PC bus to the Genie chip: IRQ2, IRQ3, IRQ5, I/OCHCK-. If IRQ3 is used by the COM2: serial port

then it is not available for use by a PC bus card. Jumper E5 is not used in the PC bus version.

Users who want to write their own interrupt service routines should note the following guidelines.

The address of the interrupt service routine should be placed in the interrupt vector table - the entry in this table consists of two 16-bit words to be placed in the Code Segment and program Counter registers. As well as ensuring the 80286 interrupts are enabled the user should ensure that the interrupt mask bit relating to the interrupt request level being used is cleared in the Genie's interrupt controller at I/O address 21H.

The interrupt service routine should clear the interrupt by performing the appropriate accesses to the I/O card causing the interrupt. At the end of the interrupt service routine an end of interrupt operation should be performed to I/O address 20H.

Users should note that for PC compatibility the interrupt controller must be programmed for edge sensitive operation, while the STEbus convention is to use open collector ATNRQn* interrupt request lines, which would normally be used as level sensitive interrupts. To ensure that interrupts which occur during the interrupt service routine are recognised by the interrupt controller the following algorithm should be used.

The code in the interrupt service routine should identify an STEbus device which is asserting an interrupt request and service that interrupt in the normal way. Then all devices which can assert an interrupt on the ATNRQn* line involved should be disabled. This is to ensure that the ATNRQn* signal goes inactive. Next the Genie interrupt controller should be reset by performing the end of interrupt operation described above. Then the interrupts on the STEbus card(s) should be turned on again. This will cause the ATNRQn* line to be asserted if there are other pending interrupt requests. Finally the 80286 interrupts should be enabled and the return from interrupt instruction executed.

5.5 DMA

The DMA mechanisms of some processors, like the Hitachi 64180, are easily adapted to the STEbus architecture, since these processors perform DMA as two distinct bus cycles - an I/O read followed by a memory write for example. The Intel DMA architecture (used by the 80286 and Genie chip) however uses a "fly-by" DMA transfer - the DMA controller performs a single memory bus cycle while asserting a DMA acknowledge signal. This is difficult to support on the STEbus since there are no DMA acknowledge signals explicitly provided.

DSP Design have proposed an extension to the STEbus specification to allow ATNRQn* signals to be used as DMA acknowledge and terminal count signals, as well as DMA requests and interrupt requests.

The ECAT can support two DMA channels on the STEbus, each using two ATNRQn* signals. The DMA channels will operate between the ECAT and STEbus slave cards which have been designed to operate with a DMA acknowledge signal. DSP Design will be introducing several such peripheral cards, such as IEEE 488 controller and a hard disk controller. The manuals for these cards will describe how to configure the ECAT for DMA operation.

Table 7 shows the ATNRQn* signals which can be used for DMA request and acknowledge signals. The TC signal is a terminal count output, required in some systems. Note that the DREQ1/DACK1- channel cannot be used on the REV B version of the ECAT. This DMA channel is available for use on the REV C PCB version.

The PC bus version of the ECAT operates DMA in the conventional manner. The following DMA signals are provided on the PC bus connector: DREQ1, DACK1-, DREQ2, DACK2-, DREQ3, DACK3- and TC. Note that DREQ2/DACK2- are used by the floppy disk controller.

6 RESET OPTIONS

A full set of reset options exist for the ECAT. The reset circuit is built around the Maxim MAX694 reset chip. This chip includes a power-supply monitor and a watchdog timer. To avoid glitches on the reset signal the MAX694 will always hold the reset signal asserted for a minimum of 200ms. This ensures all circuitry is properly reset, and conforms to the STEbus specification.

6.1 POWER SUPPLY MONITOR

The MAX694 monitors the +5V supply voltage. When the supply drops below 4.65V the MAX694 will assert the ECAT reset signal. Once the power supply returns to being within specification, the reset signal will be released after 200ms. This circuit prevents power "brown-out" causing unpredictable behaviour.

Users should note that if the voltage drop across the cables which link the power supply to the ECAT is excessive then the power supply monitor may reset the ECAT. This may also happen if there are noise spikes on the power supply.

6.2 WATCHDOG TIMER

A watchdog timer pin exists on the MAX694. The function of a watchdog timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be "kicked" and so eventually it will timeout and reset the computer.

The watchdog timer on the ECAT is optional. It is not normally implemented when the ECAT leaves the factory. If it is to be used then a resistor needs to be installed and changes needs to be made to the BIOS and address decoder. These are described below.

If the watchdog timer pin is not driven either high or low, but is allowed to float then the watchdog timer is disabled. This is the case with the standard ECAT, as shipped from the factory. If however the pin is driven, then it must be toggled regularly or the watchdog timer will timeout and the reset signal will be asserted.

If the watchdog timer is required, then a 100 ohm register must be fitted to R9. The watchdog is "kicked", or reset, by reading or writing to an I/O address in the range 320H-32FH. The I/O port must be accessed at least every 100ms, or the watchdog will time out and the ECAT will be reset (there is one exception to this - the period is 1.6 seconds

immediately following reset). Since in the standard ECAT the BIOS ROM and the address decoder PAL assign addresses 320H-32FH to the STEbus, users who want to use the watchdog timer must change both the PAL and the BIOS. Ask your dealer for details.

The standard BIOS does not perform this access of the watchdog timer. It is up to the user to write code which will do this.

One approach would be to access the watchdog timer port every tick of the MS-DOS clock, that is, approximately 18 times per second. This technique is not very robust, as it is possible for the main application program to crash but for the timer interrupt service routine to continue to function normally. Users who wish to use a more robust watchdog timer must include code in their application program to access the watchdog timer. This code should not be an interrupt service routine.

6.3 RESET SWITCH

The ECAT can be reset by pushing a reset switch.

The reset switch works by shorting the MAX694 watchdog timer pin to ground. Thus irrespective of what the watchdog timer software is doing the watchdog timer will timeout and the ECAT will be reset.

In REV B versions of the ECAT the reset switch, SW1, is located between the battery and the STEbus connector. In REV C versions the reset switch is near the 100 way connector.

Users will observe that holding the reset switch down will result in a sequence of reset pulses at approximately 1 second intervals.

6.4 RESETING THE STEbus

The ECAT can reset the STEbus, or can receive a reset from the STEbus. In the standard configuration the ECAT resets the STEbus by asserting the SYSRST* signal.

The SYSRST* signal is asserted whenever the MAX694 is driving the ECAT's on-board reset signal - that is, in response to a power failure, or watchdog timer timeout, or switch depression.

In order to drive the STEbus SYSRST* line, transistor Q5 must be installed and diode D2 must be omitted. This is the standard configuration of the ECAT.

The PC bus version of the ECAT drives the PC bus RESET

signal. There are no component options.

6.5 RESET FROM THE STEbus

The ECAT can be reset as a result of the STEbus SYSRST* signal being asserted (for instance, by a reset switch located on a front panel).

This mechanism is similar to the operation of the reset switch - that is, when SYSRST* goes low the watchdog timer begins to timeout, and a sequence of reset pulses will occur as long as SYSRST* is held low. This means, of course, that short duration pulses on SYSRST* may not be long enough to reset the ECAT.

If the ECAT is to be reset from the STEbus, then transistor Q5 should be removed and a 1N914 diode installed as D2.

The PC bus version of the ECAT cannot be reset from the PC bus.

7 ECAT-X OPERATION

A second circuit board can optionally be added to the ECAT to add extra functions. The board is called the ECAT-X and adds the the following functions:

VGA or EGA graphics
Socket for an 80287 type maths coprocessor
Second serial port (COM2:)
Circuitry to support an extra ROM disk (up to 1Mbyte)

A partially populated version of the ECAT-X, called the ECAT-X2, provides all of the extra functions except the VGA/EGA graphics.

There are three connectors on the ECAT-X. They are used as follows:

J3 COM2: serial port (RS-232 level signals).
J4 VGA graphics output (analog video plus digital sync signals).
J5 EGA and MDA graphics output (digital video).

The pin assignments of these connectors are given in Appendix F.

7.1 INSTALLING THE ECAT-X

The ECAT-X is a single Eurocard circuit board (the same size as the ECAT). It is positioned 0.8" above the ECAT and so occupies a slot in an STEbus rack. However it has no connector to the STEbus - rather all of the signals pass between the two boards through two 50-way connectors, on opposite edges of the boards. This mode of connection has two main advantages - first it allows the board set to operate stand-alone, without a backplane, and second it allows data transfers between boards to operate without any delays which backplane bus transfers would introduce.

To install an ECAT-X the following steps should be taken:

1 Disable ECAT graphics by installing both R6 and R7, or by using the partially populated versions of the ECAT which lack the graphics chips (Note this step should not be performed if fitting an ECAT-X2.)

2 Remove the jumper at E7. This jumper is located between the 80286 processor and the four resistor networks.

3 Carefully insert the pins of the ECAT-X in the corresponding sockets on the ECAT, ensuring that the pins are all properly aligned. Push the ECAT-X firmly home.

7.2 VGA AND EGA GRAPHICS

VGA and EGA graphics can be provided by the ECAT-X. EGA graphics modes provide 640 x 350 pixel resolution in 16 colours. EGA video is digital - that is the monitor is driven by TTL level digital signals. VGA graphics provides 640 x 480 or 800 x 600 pixel resolution as well as analog video - the red, green and blue signals to the monitor are analog voltages. The analog voltages are the output of a triple digital to analog convertor chip - the RAMDAC - which converts an 8-bit digital byte to one of a large number of colours (only 256 different colours can be displayed at a time).

The key to the EGA and VGA graphics is the Oak Technology OTI-037 graphics controller chip. This chip is register compatible with the IBM VGA and EGA controllers, and also provides backward compatibility with all earlier standards - MDA, Hercules and CGA.

The chip supports 256k bytes of DRAM which stores the picture information. The video memory is mapped into a 128k byte space between addresses A0000H and BFFFFH. In addition, the BIOS code for driving the enhanced graphics modes resides in an EPROM in IC2 on the ECAT-X board, at addresses C0000H-C7FFFH.

The video mode which the VGA chip is initialised to is set by the jumper area E3. Table 9 defines the settings of this jumper area. Tables F5 and F6 in Appendix F list the pin assignments of the video connectors.

GRAPHICS MODE	JUMPER SETTINGS
VGA	B1-C1, A2-B2, B3-C3, B4-C4
EGA	A1-B1, B2-C2, A3-B3, B4-C4
MDA, Hercules	A1-B1, A2-B2, A3-B3, B4-C4
CGA	A1-B1, B2-C2, B3-C3, A4-B4

TABLE 9 - DISPLAY TYPE CONFIGURATION

7.3 COM2: SERIAL PORT

A second serial port, COM2:, is provided on the ECAT-X. Actually, the UART associated with COM2: is actually on the ECAT board, in the 82C452 chip, and the ECAT-X PCB provides the RS-232 transceiver circuit and a connector for the second port.

COM2: provides the same range of serial I/O functions as

COM1: on the ECAT. Both are fully compatible with the IBM PC and AT UARTs, both at the BIOS level and the hardware level.

COM2: is able to generate interrupts to the 80286 if communications software requires it. Interrupt level IRQ3 is allocated to COM2:. If IRQ3 is to be used as an interrupt from COM2: then jumper E5 must be removed on STEbus versions of the ECAT (otherwise IRQ3 is driven by an STEbus ATNRQn* signal).

At the time of writing the BIOS does not automatically initialise the COM2: serial port following reset. The MS-DOS MODE command should be run to set baud rate etc prior to using COM2:.

The serial port is connected to external RS-232 devices through the 10 way connector J3. The pin assignments for this connector are given in Appendix F, Table F7. This allocation of pins makes it easy to connect a 9 way D-type connector to comply with the pin assignments used on the IBM AT.

7.4 80287 MATHS COPROCESSOR SOCKET

An 80287 type maths co-processor chip can be installed a socket on the ECAT-X. If this is done a 4k7 resistor must be installed in the R3 position, immediately above the 80287.

DSP Design recommend the 2C87 chip from IIT. This is a CMOS chip which is compatible with the Intel 80287, but which runs faster. The 2C87 also includes additional instructions, including a 4x4 matrix multiply. DSP Design are able to supply this chip.

The BIOS is configured to run the 80287 clock at the same frequency as the 80286 clock speed, so an 80287 of the correct speed should be chosen.

7.5 ECAT-X ROM DISK

Two sockets exist on the ECAT-X board to be used as ROM disks. Section 4.4 and 8.3 contain further information on ROM disks.

The ROM disk on the ECAT-X is implemented via the Genie chip's EMS bank switched memory registers. This allows the ROM disk to occupy none of the 1M byte memory space of MS-DOS.

The EPROM sockets are designed to take 1M bit (128k byte), 2M bit (256k byte) and 4M bit (512k byte) EPROMs. Since there are two sockets the ROM disk can be anywhere between 256k bytes and 1M byte.

The sockets are also designed to take 1M bit Flash EEPROMs. These are EPROMs which can be erased electrically, thus allowing non-volatile read-write memory. Flash EEPROMs typically require a high voltage (of around 12.5V) for the writing operation. This must be provided from an external power source, through jumper E1. Support will soon be provided in the ROM disk driver for EEPROMs.

Users will not normally need to know the mechanism by which the EPROMs are accessed, as this is handled automatically by the ROM disk software. If this information is required, contact your dealer.

There are two jumpers on the ECAT-X which are associated with ROM disks. These are E1 and E2, and they are discussed in Appendix B.

8 SOFTWARE

The ECAT offers a very high degree of PC compatibility. The vast majority of software (both operating systems and applications software) which will run on on IBM PC/AT will also run satisfactorily on the ECAT.

Section 1.3 contains a discussion on AT compatibility.

Most users will wish to use the MS-DOS operating system (booting from a hard disk, floppy disk or ROM-disk) and then run off the shelf software, or their own application. DSP Design offers a number of software products to ease software development.

8.1 BIOS ROM

The BIOS is a program which interfaces between the ECAT hardware and the operating system and application code. It is responsible for controlling the ECAT hardware, and providing a standard interface to the higher levels of software. The BIOS also deals with functions such as initialisation and testing the ECAT hardware following power-on.

The ECAT uses a BIOS supplied by American Megatrends Inc (AMI). The BIOS is stored in a 64k byte EPROM, which is plugged into the IC12 socket. DSP Design have added some enhancements to the BIOS. Users should note that the BIOS is copyright American Megatrends Inc and DSP Design and may not be copied.

The ECAT software and options are continually being enhanced. As time goes on new features are being introduced into the BIOS, allowing for more disk drives, display modes etc. Some of the disk drive and memory map options may require different BIOS ROMs. If you have a non-standard configuration you should check that you are receiving the correct BIOS when you order your system. In particular, a different BIOS is required for systems which are using a SCSI disk drive.

8.2 MS-DOS

The ECAT will run any version of MS-DOS (except those which Microsoft have deliberately prevented from running on an 80286 processor). The computer will boot MS-DOS from a floppy disk, from a hard disk or from a ROM disk.

DSP Design supply Microsoft's MS-DOS 4.01 operating system. As part of our license agreement with Microsoft we have negotiated the right to blow this MS-DOS into EPROM, for use with ROM disk systems. Users should note that most copies of

MS-DOS obtained from other sources may not legally be run on the ECAT, or blown into EPROM, under the terms of the Microsoft license agreement. Bootleg copies of the operating system of course may not be run on the ECAT.

In systems which boot from floppy disk, an MS-DOS boot disk should be inserted in the A: floppy disk drive. DSP Design's MS-DOS usually comes on 3.5" disks, but it can be supplied on 5.25" disks on request.

MS-DOS can be transferred to a hard disk for users who want to boot from hard disk. Details of configuring a hard disk system are given in section 4.7.

The final option will prove attractive for users who want an entirely solid-state PC. In this option MS-DOS can be programmed into an EPROM, which is referred to as a "ROM disk". Conceptually the ROM disk is the same as a read-only floppy disk - it can be used to store programs and data files as well as the operating system. Following power-on the ECAT will load the operating system from the EPROM, and with a suitable AUTOEXEC.BAT file the user's application program will then be loaded and executed.

8.3 ROM DISK

A "ROM disk" can be implemented on the ECAT. This is on EPROM which is configured (by the BIOS) to appear as a disk drive. Program and data files, and the MS-DOS operating system itself, can be stored in the ROM disk just as though it were a floppy disk. Having a ROM disk in the system still allows the use of floppy disk drives. Section 4.3 discusses ROM disk options.

Programming the ROM disk is done with an EPROM programmer and utility software supplied by DSP Design. The ROM disk software is supplied on an ECAT Utilities disk (part number ECAT-UTIL) on a 3.5" floppy disk. DSP Design can supply the software only, or the EPROMs as well. Alternatively, a ROM disk programming service is provided - ask your dealer for details.

The procedure for creating a ROM disk is given below. This assumes that you are running the ROM disk generation software on a desk top PC with a hard disk as C: and a floppy as A:.

1 Creating the floppy

Copy the files you want in the ROM disk onto a freshly formatted floppy disk. If your ROM disk is to contain MS-DOS you should format the disk using the /s option, to copy the MS-DOS files onto the disk. Once the disk has been formatted

you should not erase any files, since this will fragment the data on the disk.

To check that your files will fit on your EPROMs by running the MS-DOS CHKDSK program. The EPROM space required is the difference between the "total disk space" and the number of "bytes available on disk". Use a 360k or 720k disk format if possible since less space is allocated on smaller disks to directories and file allocation tables.

You should test your disk performs as expected by running it in in the target system with the write protect enabled.

2 Making a binary image

Run the program MKDOSVOL to create a binary image of the floppy disk. This program has two parameters:

[d:\path\]filename
This defines the file to which the ROM image is written. Note you must not use a file extension for the file name - eg call you file "image", not "image.rom".

[d:drive]
This optional parameter is the physical unit number of the floppy drive to read the ROM image from - ie 0 for drive A:. The default is unit0, drive A:.

An example of running this program is:

```
MKDOSVOL MYIMAGE
```

This will create a file called MYIMAGE in the current directory on C: from the floppy in A:.

3 Breaking the image into smaller files

The next step is to break the ROM image into blocks suitable for downloading to EPROM programmers. The program FB32 will generate 32k byte files from the file produced by MKDOSVOL, and the program FB64 will create 64k byte files. To run either of these utilities type the command name followed by the name of the ROM image file.

For example:

```
FB64 MYIMAGE
```

This will create a sequence of 64k byte files called MYIMAGE.001, MYIMAGE.002 etc. These binary image files can be down loaded to the PROM programmer, either in their binary form, or as HEX files if they are converted from binary to HEX by a suitable utility.

4 Generating a driver

Before blowing the PROMs you will need to generate a ROM disk driver to match the ROM disk you are going to be using. This is done by running the MKECROM program. MKECROM leads you through a number of steps and results in the generation of a file called ECROM.BIN, which is a version of the ROM disk driver which is customised for the particular set of drive letter allocations you require for you system. The drive letter allocation options are discussed in detail in section 4.2.

5 Assembling the components and blowing an EPROM

You now have the elements that you need to assemble into a ROM disk. To recap - these are the various 32k or 64k byte files containing the floppy image, the ROM disk driver, and the ECAT BIOS itself, which is contained in the 64k byte EPROM which is shipped with the ECAT.

These elements need to be assembled in the correct order in the EPROM programmer and blown into an EPROM or EPROMs. The arrangement of these elements is best done in the EPROM programmer itself, and the details of this depends on the programmer. The rules are as follows:

The ECAT BIOS must remain at the same address as it normally is - that is the 64k bytes from F0000 to FFFFF.

The ECROM.BIN file produced by MKECROM is actually a program which is found during the BIOS ROM search process shortly after reset. As such it must be located on a 2k byte boundary somewhere in the address range A0000H to EB800H (but not in the range EC000H-EFFFFH, as this is where the EMS window is located for ECAT-X ROM disks). ECROM.BIN is 2k bytes in size.

If the ROM disk is a "flat" ROM disk, that is it appears permanently in the memory space of the ECAT, then the image files must be located starting at the address allocated to them by the MKECROM program.

If the ROM disk is an ECAT-X ROM disk then the image files must be split into odd and even bytes and placed at the beginning of the EPROMs occupying IC1 and IC8 on the ECAT-X board.

Two examples will serve to demonstrate the positioning of the files in the EPROM.

In the first case a 256k byte EPROM is to contain the BIOS, a ROM disk and the ROM disk driver. The best way of doing

this is to down-load to the programmer the image files and blow them into EPROM starting at offset 800H in the EPROM. Space must be left for the 2k byte ECROM.BIN file which should be programmed at address 0 (filling the space up to 7FFH), and then the BIOS EPROM should be read by the programmer and blown into the EPROM at offset 30000H.

In the second case 512k byte ECAT-X ROM disk is used, occupying two 256k byte EPROMs. In this case the image files are split into odd and even bytes and programmed into the two EPROMs, starting at offset 0. No space is required for the ECAT BIOS or for the ECROM.BIN driver. Instead, the BIOS is left as it was, in IC12, and a second small EPROM is used just for the driver. The ECROM.BIN file is programmed into this EPROM at any 2k byte boundary within the ranges noted above.

Care should be taken when blowing EPROMs of size n bytes which do not begin on a n byte boundary. An example of this is a 128k byte EPROM starting at address 90000H. If you consider the most significant address bit of the EPROM (A17) you will see that this is a 1 at addresses 90000H-9FFFFH (the "first half" of the ROM disk) and a 0 at addresses A0000H-AFFFFH (the "second half" of the ROM disk). As a consequence the first 64k bytes of the ROM disk binary image files must be programmed into the second half of the EPROM, and vice versa.

Users should also note that the ECROM.BIN file may not be placed in a 27011 bank switched EPROM, nor in the ECAT-X ROM disk, since the driver will "vanish" when other banks are selected. (At the time of writing the 27011 bank switched EPROMs are not supported but they should be soon).

6 Using the ROM disk

When the EPROMs have been blown they are simply plugged into the appropriate sockets on the ECAT and ECAT-X and the computer is powered on. Ensure that you have selected an appropriate address map PAL to support the devices that you are using, and that you have set the jumpers correctly for the type of devices installed.

When booting from a ROM disk the ROM disk driver will print a sign on message and invite you to type a key to select the alternate disk drive allocation. If the correct key is not pressed within a few seconds of the message then the default drive letter allocation is chosen and booting proceeds.

8.4 RAM DISK

RAM disks can also be implemented on the ECAT. These are similar in concept to ROM disks except that, being

implemented in RAM they area read-write disks rather than read-only disks. A further difference is that the ROM disk driver is effectively an extension to the BIOS, while the RAM disk driver is a loadable device driver, loaded from disk by MS-DOS.

Actually, there are two different RAM disk drivers which are available on the ECAT. The first is the RAMDRIVE.SYS driver which is provided by Microsoft with every copy of MS-DOS. This driver takes a portion of the main DRAM memory for the RAM disk, and as such it is volatile - that is, data stored in the RAM disk will be lost when the computer is reset. This driver is not recommended by DSP Design, but it is available to the user, and documented in the MS-DOS manuals.

The second RAM disk driver is supplied by DSP Design for use with Static RAM. This driver implements the RAM disk in a memory device (usually the IC11 socket or SM256 memory board) which is battery-backed up and so the RAM disk is non-volatile, and its contents remain intact after the computer is reset and the power turned off.

Both of these RAM disk drivers are supplied as loadable device drivers, rather than being incorporated stored in EPROM like the ROM disk drivers. An entry is made in the CONFIG.SYS file if RAM disks are to be used.

The DSP Design static RAM disk driver takes the from of a loadable device driver, called ECRAM.SYS. The device driver is a file which is placed in the root directory of the boot disk and which is invoked by a command in the CONFIG.SYS file. The driver program is provided on the ECAT utilities disk, part number ECAT-UTIL.

There are two files associated with DSP Design's RAM Disk - the driver itself, called ECRAM.SYS, and a formatting and status program called ECRAM.EXE.

The driver is installed in the CONFIG.SYS file as an entry in the following form:

```
DEVICE=ECRAM.SYS /a /n
```

The parameter "a" defines the starting address of the RAM disk and the parameter "n" defines the number of 32k byte blocks which are used by the RAM disk. As an example, a 128k byte RAM disk at addresses D0000H - EFFFFH is implemented with the following entry:

```
DEVICE=ECRAM.SYS /D /4
```

You can implement more than one RAM disk by making more than one entry in the CONFIG.SYS file. Each new entry implements a new RAM disk. To add to the first RAM disk a second 32k byte RAM disk at address C8000H you would includes these

entries in the CONFIG.SYS file:

```
DEVICE=ECRAM.SYS /D /4
DEVICE=ECRAM.SYS /C8 /1
```

(Note that RAM disk starting on an odd 32k byte boundary have C8, D8 etc as their address parameter. Note that 32k byte boundary RAM disks are not available at the time of writing). The two RAM disks would be allocated two drive letters - the next two available following ROM disks, SCSI disks and floppy disks.

The ECRAM.EXE program can be run from the MS-DOS command line. It allows the user to format the RAM disks, and can also report on the size and status of RAM disks. It can be run in four three ways. Use:

ECRAM	to display status of all RAM disk drives
ECRAM d:	to display status of RAM disk drive d:
ECRAM d:/F	to format RAM disk drive d:
ECRAM d:/F /P	to format drive d: with parameters (not usually used - the program will prompt you for various parameters).

The status reported by ECRAM.EXE is the size of the RAM disk and whether or not it is formatted. The format options ask whether you are sure you want to format the disk, and if so the disk is formatted ready to accept new data. All files previously stored on the disk will be erased.

Examples of using the ECRAM.EXE program are:

ECRAM C:	this will report on the size of RAM disk drive C:
ECRAM C:/F	this will format the RAM disk drive C:

Both the ECRAM.SYS driver and the ECRAM.EXE program produce a number of self-explanatory status messages.

All MS-DOS functions that work on floppy and hard disks will behave as expected with RAM disks (with the exception of rmatting commands). In particular the CHKDSK command can be used to display information about about the number of files etc. Similarly subdirectories can be created on the RAM disks, and files can be protected and hidden using normal DOS commands.

Don't forget that the data will only remain in the RAM disk while the battery power is applied, so ensure that the RAM disk is not corrupted by shorting pins on the board - for instance by putting the board down on a conductive surface or metal object. Similarly adequate plans should be taken at the system design stage to back-up data and to allow for recovery from accidental data loss, just as you would do

with a system based on mechanical disks. If the RAM disk is corrupted the driver will detect a checksum error and report the corruption with an error message.

The ECRAM RAM disk driver may be enhanced at a later date to allow it to be used with Expanded Memory DRAM. The enhanced driver would use the Genie EMS registers to convert DRAM above the 640k limit into RAM disk. This RAM disk would be volatile, and data would be lost if the power is switched off.

8.5 EMS DRIVER

It is in principle possible to use DRAM beyond the 640k byte boundary as Expanded Memory. To do this an Expanded memory device driver is needed. The device driver is invoked by an entry in the CONFIG.SYS file, just as the RAM disk drivers are.

At the time of writing an EMS driver is not available for the ECAT. One may become available in due course. If you would like an EMS driver please ask your dealer.

8.6 APPCOM SOFTWARE SUITE

A powerful development system and operating system is available for the ECAT. Called Appcom, it provides both a powerful development and debugging environment, and a easy to use kernel for the imbedded target system, in place of MS-DOS.

As a development tool, an EPROM in the ECAT containing the PROMDOS monitor program communicates to a PC-based development system via an RS232 link. The user edits and compiles code on the PC (or more likely AT) machine and downloads files to the ECAT. The PROMDOS emulates a MS-DOS environment on the ECAT (MS-DOS is not required on the ECAT). As well as providing RAM and ROM disks on the ECAT, PROMDOS also emulates MS-DOS and BIOS function calls, greatly simplifying software development.

When the application program has been debugged it is blown into an EPROM and the link to the PC development computer is removed. The PROMDOS ROM is still present on the ECAT, providing an emulated MS-DOS environment.

The key to the power and ease of use of Appcom is the fact that PROMDOS has been written specifically for real-time imbedded applications. The Appcom functions are all re-entrant and so can be called by interrupt-driven device drivers. The interrupt support means that Appcom is effectively multi-tasking.

A wide range of device drivers exist for STEbus I/O cards (serial, parallel, A/D etc). Communication with drivers is usually via high level ACSII commands (eg "BAUD=9600"). The use of these drivers greatly reduces the time and hence the expense of getting STEbus applications running.

Ask your dealer or DSP Design about the Appcom software suite.

APPENDIX A SPECIFICATION

Product: ECAT

Description: Single Eurocard PC.

Processor: 80286 running at 12.5MHz or 16Mhz.

Maths Coprocessor:
80287 type at 12.5 or 16MHz on ECAT-X board.

Memory: 512k, 1M, 2M or 4M DRAM, two sockets for byte-wide EPROM or RAM (to 512k bytes each max.) BIOS EPROM is 64k bytes.

Graphics: MDA, Hercules, CGA, Double scan CGA. VGA, EGA with ECAT-X board.

Floppy disk: Controller for two 3.5", 5.25"drives. Disks up to 1.44Mbyte capacity supported.

Printer port: Centronics compatible (PRN:). Bidirectional.

Serial interface:RS232 (COM1:), COM2: available with ECAT-X.

Keyboard port: IBM AT compatible (Scan Code Set 1 required)

Speaker port: IBM AT compatible.

Reset circuit: Push switch, power supply monitor, watchdog timer, STEbus.

STEbus interface:
Default bus master. Fully conforms to IEEE 1000 specification.

PC bus interface:
Provides all standard (eight bit) PC bus signals. (Order PC bus version of the ECAT).

Interrupts: Four incoming interrupts. Vector interrupts fetch cycles supported on STEbus.

DMA: Two DMA request/acknowledge pairs.

Connectors: DIN41612C, with rows A and C fully populated (STEbus connector), 64 pin header (PC bus connector), 100 way male right angle connector with two 50 way flat ribbon cables (peripherals).

Dimensions: 100mm * 160mm (single Eurocard) PCB, overall dimensions (including connectors): 175mm * 100mm * 10mm.

Weight: 190g approx.

Operating temperature:
0 - 70 degrees C.

Humidity: 10% - 90% non-condensing.

Power Supplies: (ECAT @12.5MHz, 1Mbyte DRAM)
+5V @ 580mA typical
For ECAT-X add 325mA typical
For ECAT-X2 add 50mA typical
For an ECAT with a CMOS 80C286 subtract approx 250mA

APPENDIX B SET-UP PROCEDURE

The component placement diagram in Appendix C may be of help in locating components referred to in this appendix.

ECAT CONFIGURATION

JUMPERS

E1 **Normally no jumper fitted.** Fit a jumper only when the floppy disk controller is omitted and a 16MHz oscillator is required for the STEbus SYSCLK signal or for monochrome graphics.

E2 **Calendar/clock battery.** This jumper connects the battery to the calendar/clock circuit. It is usually removed for shipping or storage to conserve battery life. The jumper must be fitted for the calendar clock to work, and the calendar/clock must be set up with the correct time and date after the jumper is replaced.

E3 **Memory Socket Configuration.** This socket must be correctly configured for the memory devices in IC11 and IC12. See Appendix E for details.

E4 **Factory Fitted.**

E5 **IRQ3 Interrupt Source.** This jumper should be fitted if the IRQ3 interrupt request is to come from the STEbus. It should be omitted if IRQ3 is driven by the COM2: serial port, or for the PC bus version of the ECAT.

E6 **STEbus SYSCLK.** Install link if the STEbus SYSCLK is to be driven by the ECAT, and remove the link otherwise.

E7 **ECAT-X Configuration.** Install this link if the ECAT-X expansion board is not fitted. Remove the link if the ECAT-X is fitted.

E8 **Graphic Clock Source.** This sets the dot clock frequency for the on-board graphics chip. It should be set as follows:

MDA/Hercules (Mono)	Link 4-5 (the bottom two pins)
CGA (Colour)	Link 3-4 (the second and third pins from the bottom)
Double Scan CGA	Link 1-2 (the top two pins)

E9 **Factory Fitted.**

RESISTORS

R6 and R7 can be fitted or omitted according to the desired video mode, as follows:

MDA/Hercules	Fit R7, omit R6
CGA	Fit neither
Double Scan CGA	Fit R6, omit R7
Disable ECAT graphics	Fit R6 and R7

R9 should be fitted with a 100ohm resistor if the watchdog timer is required. In addition a new address decoder PAL and BIOS will be required. Ask for further information.

ECAT-X CONFIGURATION

JUMPERS

E1 **Normally Fitted.** Remove jumper and supply EEPROM programming voltage to pin 2 of this connector if EEPROMs are to be programmed in situ.

E2 **EEPROM Selection.** Use position 2-3 for 4M bit (512k byte) EPROMS in IC1 and IC8. Use position 1-2 for EEPROMs. For 1M bit (128k byte) and 2M bit (256k byte) EPROMs this jumper should be omitted. REV B versions of the ECAT-X will need a 10k pull-up resistor between pins 31 and 32 of IC1 to operate with 1M and 2M bit EPROMs.

E3 **Graphics Mode.** This jumper area selects the graphics mode of the ECAT-X graphics sub-system. Position jumpers as follows:

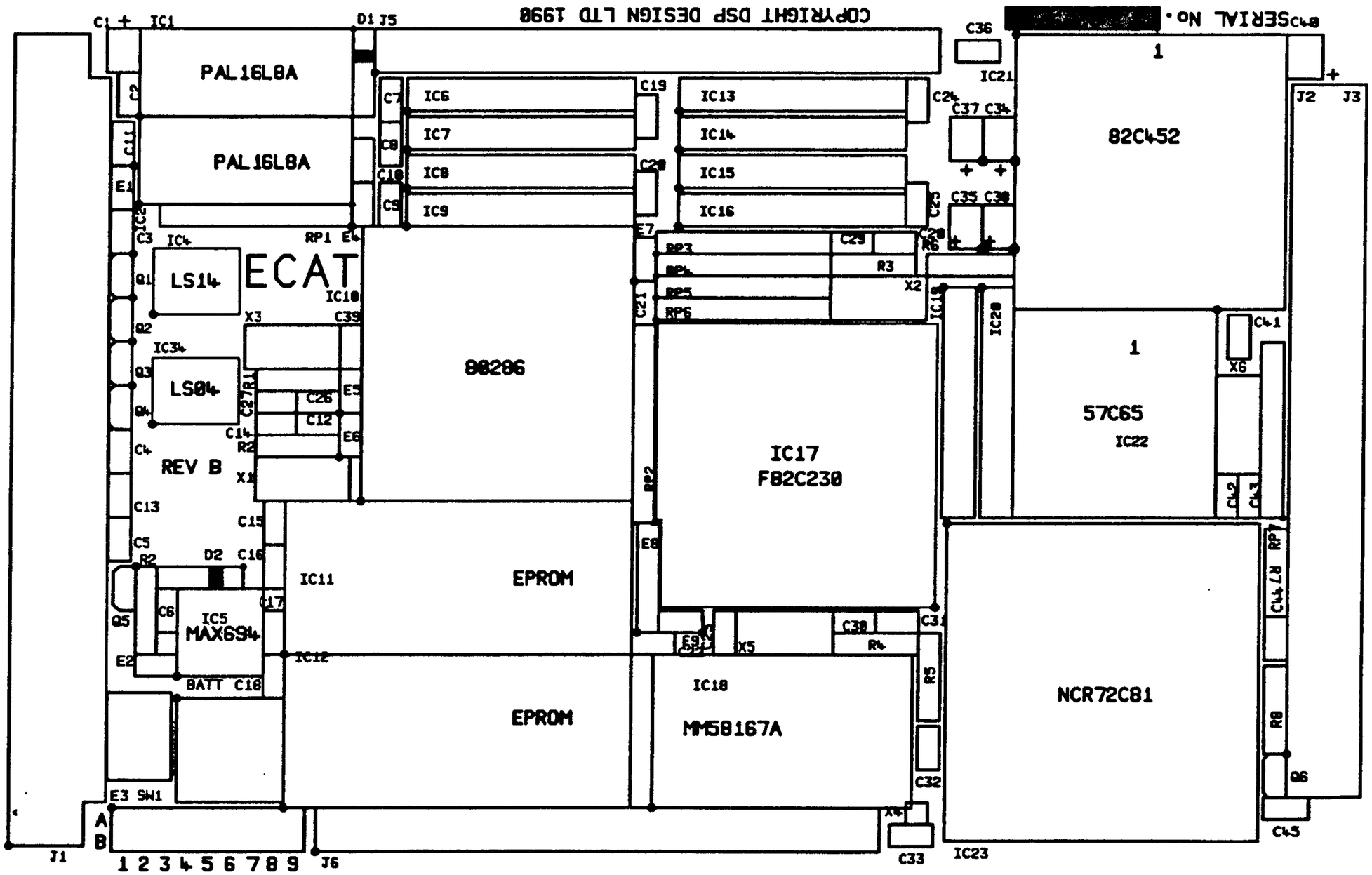
VGA	B1-C1, A2-B2, B3-C3, B4-C4
EGA	A1-B1, B2-C2, A3-B3, B4-C4
MDA	A1-B1, A2-B2, A3-B3, B4-C4
CGA	A1-B1, B2-C2, B3-C3, A4-B4

APPENDIX C COMPONENT PLACEMENT DIAGRAM

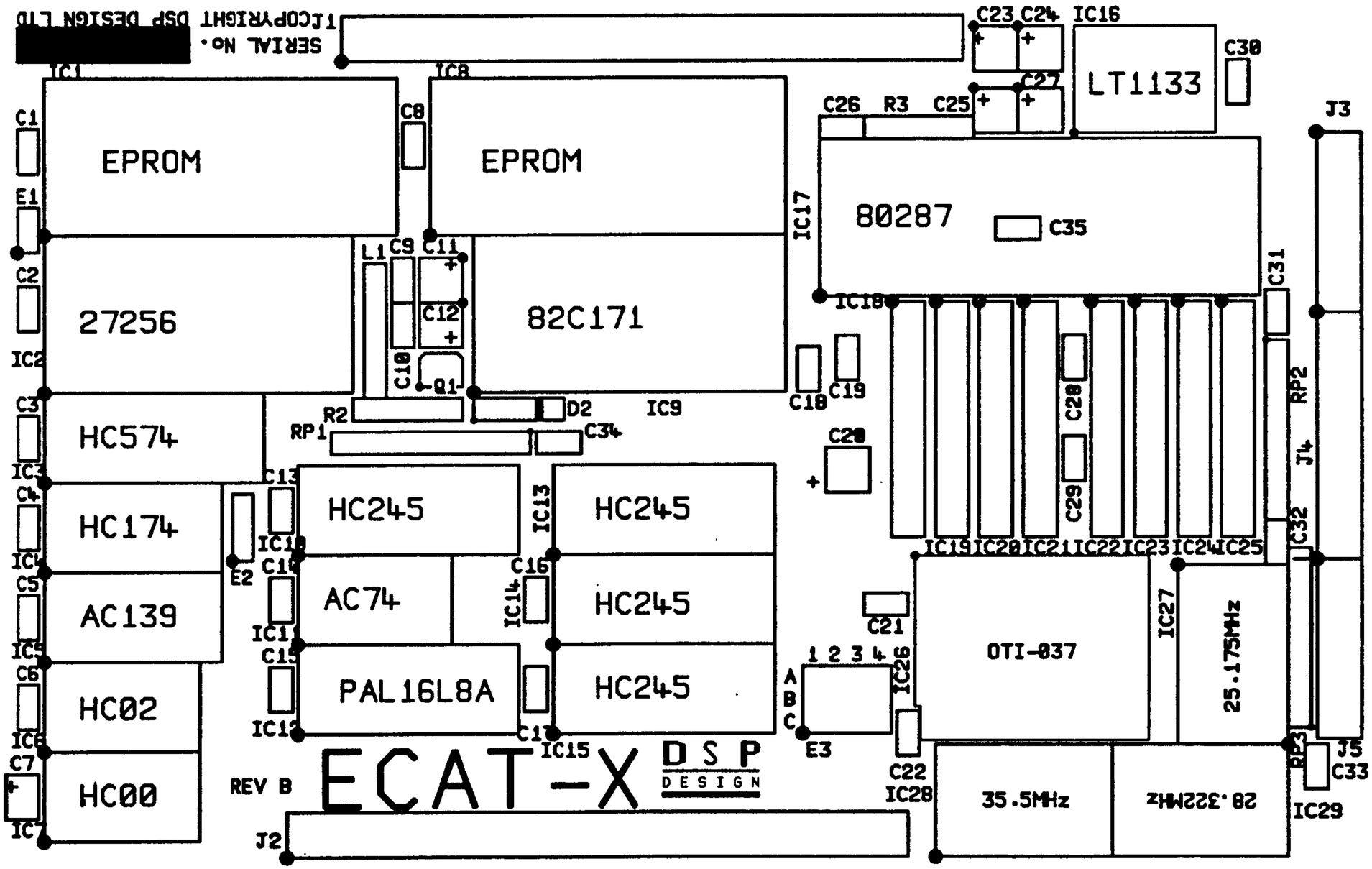
The two component placement diagrams which follow may be of help in locating the components referred to in Appendix B.

As a guide to curious users, some of the key components of the ECAT are identified here:

IC1	Address Decoder PAL
IC2	Bus Interface Timing PAL
IC6-98,13-16	Main DRAM memory (256k x 4 chips)
IC10	80286 microprocessor
IC11	Socket for EPROM or SRAM
IC12	BIOS EPROM
IC17	Genie chip
IC18	Calendar/Clock chip
IC21	Serial and Parallel I/O controller
IC22	Floppy disk controller
IC23	Graphics controller
IC19, 20	Video memory


COPYRIGHT DSP DESIGN LTD 1990
SERIAL No.
PAL16L8A
PAL16L8A
IC1
D1
J5
IC6
IC7
IC8
IC9
IC13
IC14
IC15
IC16
C19
C20
C36
IC21
C24
C37
C34
C35
C38
C25
C26
R6
82C452
J2
J3
C41
X6
1
57C65
IC22
RP1
E4
IC4
LS14
ECAT
IC10
X3
C39
IC34
LS04
C27
R1
C26
E5
C12
C14
R2
E6
REV B
X1
C13
C15
C5
D2
C16
R2
IC11
EPROM
C17
C6
IC5
MAX694
Q5
E2
BATT
C18
IC12
EPROM
00286
RP3
RP4
RP5
RP6
C29
R3
X2
C21
E7
IC17
F82C230
E8
X5
R4
IC18
MM58167A
C31
C32
R5
NCR72C81
IC23
C33
X4
RP7
C44
R7
R8
Q6
C45
E3
SW1
A
B
1 2 3 4 5 6 7 8 9
J1
J6

C2



C3

LAYER 7 COMPONENT LEGEND

APPENDIX D ECAT OPTIONS AND ORDERING INFORMATION

The ECAT is very flexible in terms of components which can be fitted or omitted from the board. In this way the ECAT can be optimised for price and performance.

Some of the options are offered as standard items - that is options which can be ordered for small orders of ECAT cards. Other configurations may be possible for larger quantities by special arrangement with DSP Design. Contact your dealer for details.

STANDARD ITEMS

ECAT01	Single Eurocard AT with 512k DRAM
ECAT02D	ECAT01 without disk controller
ECAT03G	ECAT01 without graphics controller
ECAT04C	ECAT01 without disk or graphics controller
ECAT03GX	ECAT03G with ECAT-X fitted
	Append -1 to part numbers for 1M byte DRAM
	Append -2 to part numbers for 2M byte DRAM
	Append -4 to part numbers for 4M byte DRAM
	Append -PC to part numbers for PC bus interface
	Change ECAT- to ECAT-C- for a version with a CMOS 80C286 processor
	Append -16 for the 16MHz version
ECAT-X	Expansion card - fully populated
ECAT-X2	Expansion card - no graphics
ECAT-BP	Cable assembly, 3U aluminium panel, all PC connectors for ECAT
ECAT-BPX	Cable assembly, 3U aluminium panel, all PC connectors for ECAT and ECAT-X
ECAT-CA	Cable assembly - 100 way connector and cable only
ECAT-MSDOS	Microsoft MS-DOS 4.01 Operating System
ECAT-UTIL	Utilities disk incl. ROM disk generation program and RAM disk driver

ACCESSORIES

KEY-10	PC compatible keyboard - commercial grade
KEY-20	PC compatible keyboard - industrial grade
MNM-14	Monochrome monitor - green, 14"
CLM-14	Colour monitor - CGA, EGA, VGA 14"
ECATSYSX42-5	ECAT03GX, ECAT-BP, DIS35-3U mounted in a KM7 rack 9.5" wide with 5 slot backplane and 55W

	power supply fully wired and configured
ECATSYSX84-5	As ECATSYS42-5 with 19" rack and 75W PSU
DIS35	1" high 3.5" floppy disk drive, +5V only
DIS35-3U	DIS-35 with 3U rack fitting kit
DIS525	1" high 5.25" floppy disk drive, +5V only
HD32	32M byte 3.5" SCSI drive
STE-DISK	DIS-35 mounted on plug-in STEbus board
PPL-3	Powerplane - power supply and 3 slot backplane
PT-1	Powerterm - power supply and terminator to convert ECAT to standalone operation

BAT32D	32 pin battery back-up socket
EPROM32	32k byte EPROM
EPROM128	128k byte EPROM
EPROM256	256k byte EPROM
RAM32	32k byte SRAM
RAM128	128k byte SRAM

APPENDIX E ALTERNATIVE MEMORY MAP OPTIONS

Since the address decoding is done by PAL, other address maps are possible. There are already quite a number of address decoding PALs for the ECAT, and it is possible to design others if the existing PALs do not give the required address map. This appendix summarises the characteristics of each of the existing address decoding PALs. The PALs are fitted in the socket marked IC1.

The tables below can be interpreted as follows:

The left hand column represents a 64k byte address range - for example "F" represents the addresses from F0000H-FFFFFH.

The next columns are headed "ADR2", "ADR6" etc. This is shorthand for the name of the address decoder PAL - ADR2 for instance represents the PAL called ECATADR2.

The entries in the columns below the name of the device represent the memory device which occupies the associated memory locations:

IC12	This is the first of the bytewide memory sockets.
IC11	This is the second of the bytewide memory sockets.
STEbus	Accesses to these addresses are performed to the STEbus memory address space.
VIDEO	These addresses are to the on-board graphics controller chip.
DRAM	This is the on-board DRAM memory.

The PALs ECATADR2 and ECATADR6 are special cases. With both of these PALs IC11 and IC12 each occupy 32k bytes. IC12 is present in the range F8000H-FFFFFH and IC11 is present in the range F0000H-F7FFFH.

Those memory maps with two entries in the region C0000-CFFFF have the ECAT-X BIOS occupying the lower 32k bytes and the other memory device occupying C8000-CFFFF.

In all other cases the boundaries between each type of memory occurs on a 64k byte boundary, although the address decoder PAL is capable of a resolution of 32k bytes.

Tables towards the end of this appendix give information on correct configuration of the E3 jumper area.

	ADR2	ADR6	ADR7	ADR8	ADR9	ADRB	ADRC	ADRE
F	IC11,12	IC11,12	IC12	IC12	IC12	IC12	IC12	IC12
E	STEbus	STEbus	IC11	IC12	IC12	IC12	IC11	IC11
D	STEbus	STEbus	STEbus	IC11	IC11	IC12	STEbus	STEbus
C	STEbus	STEbus	STEbus	IC11	STEbus	IC12	STEbus	STEbus
B	VIDEO	VIDEO	VIDEO	VIDEO	VIDEO	VIDEO	VIDEO	STEbus
A	STEbus	STEbus	STEbus	STEbus	STEbus	VIDEO	VIDEO	STEbus
9	STEbus	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
8	STEbus	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
7	STEbus	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
6	STEbus	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
5	STEbus	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
4	STEbus	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
3	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
2	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
1	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
0	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM

EIGHT OF THE ECAT ADDRESS DECODER PAL ADDRESS MAPS

	ADRF	ADRI	ADRJ	ADRL	ADRM	ADRN	ADRS	ADRX
F	IC12	IC12	IC12	IC12	IC12	IC12	IC12	IC12
E	IC11	STEbus	IC11	IC12	IC12	IC12	IC12	IC11
D	STEbus	STEbus	STEbus	IC12	IC12	IC12	IC11	IC11
C	STEbus	STEbus	STEbus	IC12	IC12	IC12	STEbus	VID,STE
B	STEbus	VIDEO	VIDEO	VIDEO	VIDEO	VIDEO	STEbus	VIDEO
A	STEbus	IC11	STEbus	STEbus	IC11	STEbus	STEbus	VIDEO
9	STEbus	IC11	STEbus	IC11	IC11	STEbus	STEbus	DRAM
8	STEbus	STEbus	STEbus	IC11	STEbus	IC11	STEbus	DRAM
7	DRAM	DRAM	DRAM	DRAM	DRAM	IC11	STEbus	DRAM
6	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	STEbus	DRAM
5	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	STEbus	DRAM
4	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	STEbus	DRAM
3	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
2	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
1	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM
0	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM

EIGHT OF THE ECAT ADDRESS DECODER PAL ADDRESS MAPS

ECAT MEMORY DEVICE SELECTION

The ECAT has two sockets for byte wide memory devices. IC12 is always an EPROM (it contains the bootstrap code and BIOS). IC11 can contain an EPROM, RAM or bank switched EPROM.

The jumper area E3 is used to select the type of memory devices installed in the IC11 and IC12 sockets. To prevent the numbers of pins at these jumper areas becoming excessive, some restrictions have been placed on the type of memory devices which can be fitted in the two sockets. IC12 can contain an EPROM, and IC11 can contain an EPROM of the same size as IC12, or a RAM chip, or a bank switched EPROM. (other EPROM sizes for IC11 may be possible). This is summarised below.

IC12 - ALLOWABLE MEMORY DEVICES

32k byte EPROM	eg 27C256	
64k byte EPROM	eg 27C512	
128k byte EPROM	eg 27C1001	
256k byte EPROM	eg 27C2001	
512k byte EPROM	eg 27C4001	(REV C only)

IC11 - ALLOWABLE MEMORY DEVICES

No memory chip
EPROM of the same size as IC12 (see below)
32k byte or 128k byte Static RAM
Intel 27011 bank switched EPROM
Some EPROMs of other sizes may be possible.

The following tables define the jumper positions for each of these options. REV B versions of the ECAT implement only columns 1-9, and cannot support 512k EPROMs.

IC12 MEMORY DEVICE	FIT LINKS TO E3 AS FOLLOWS:
32k byte EPROM	A8-A9 and B8-B9
64k byte EPROM	A8-A9 and B7-B8
128k byte EPROM	A8-A9 and B7-B8
256k byte EPROM	A7-A8 and B7-B8
512k byte EPROM	ask your dealer

IC11 MEMORY DEVICE	FIT LINKS TO E3 AS FOLLOWS:
EPROM (same as IC12)	A3-A4, A5-A6, B3-B4 and B5-B6
Static RAM	A2-A3, A4-A5, B2-B3 and B4-B5
27011 banked EPROM	A3-A4, A5-A6, B2-B3 and A1-B1

Note that a PCB tracking error affecting boards shipped before 7 July 1990 means that people who want to use EPROMs in the IC11 socket must add a wire link between pins B6 and B8 of jumper area E3.

Some users may want to fit other combinations of memory devices in IC11 and IC12. In particular, it may be possible to find a set of jumper positions which allow EPROMs of different sizes to be used in the two sockets. To assist such users, the following table describes the use of the various pins of E3. This table should be used in conjunction with the pin assignments of the memory chips to determine a suitable set of jumper positions.

E3 PIN ROW A	CONNECTS TO:	E3 PIN ROW B	CONNECTS TO:
A1	+5V	B1	IC11 pin 3
A2	Processor A15	B2	Processor WR
A3	IC11 pin 31	B3	IC11 pin 29
A4	+5V	B4	Processor A14
A5	IC11 pin 30	B5	IC11 pin 3
A6	IC12 pin 30	B6	IC12 pin 3
A7	Processor A17	B7	Processor A15
A8	IC12 pin 30	B8	IC12 pin 3
A9	+5V	B9	+5V
A10	IC12 pin 31	B10	Processor A18
A11	IC12 pin 31	B11	Processor A19

APPENDIX F CABLE PIN ASSIGNMENTS

The ECAT has connectors to I/O devices (disk drive, keyboard etc) and to the expansion bus (either the STEbus or the PC bus). The I/O connections are made through a 100 way connector which in turn mates with a cable assembly containing two 50-way ribbon cables on standard pitch (0.05 inch). The bus connections are made either through a DIN-41612-C connector (in the case of the STEbus) or a 64 way straight pin header (in the case of the PC bus).

The ECAT-X has three connectors for its video and serial ports.

Descriptions and pin assignments of all of the connectors are given below.

ECAT PERIPHERAL CONNECTORS

The peripheral devices are connected to the ECAT through a 100 way connector, called J2. The 100 pins on the connector are brought to the outside world through two 50-way ribbon cables. The bottom cable is for the floppy disk drive and power supplies, and the top cable is for everything else.

In this context the "top" and "bottom" cables are defined as follows. Place the ECAT board on a table with the EPROM sockets face up and J2 cable assembly plugged into the ECAT (with the strain relief clip present on the connector). If the STEbus or PC bus connector is to the left then the two 50-way ribbon cables stretch out to the right, one on top of the other. The "top" cable is defined as the upper-most cable and the "bottom" cable is the cable closest the table.

The tables of pin assignments which follow list the signal name and also the peripheral to which the signal belongs and the pin number of that peripheral's connector. The peripherals use the following connectors:

Centronics Printer:	25 way female D-type
Keyboard:	5 way female circular DIN
Serial:	9 way male D-type
Video:	9 way female D-type
Loudspeaker:	Speaker wired direct to cable
Floppy Disk Drive:	34 way female IDC connector
Disk Power Supply:	4 way Molex

J2 PIN	SIGNAL	CONNECTS TO: PERIPHERAL	PIN
1	STROBE-	CENTRONICS	1
3	D0	CENTRONICS	2
5	D1	CENTRONICS	3
7	D2	CENTRONICS	4
9	D3	CENTRONICS	5
11	D4	CENTRONICS	6
13	D5	CENTRONICS	7
15	D6	CENTRONICS	8
17	D7	CENTRONICS	9
19	ACK-	CENTRONICS	10
21	BUSY	CENTRONICS	11
23	PE	CENTRONICS	12
25	SELECT	CENTRONICS	13
27	GND (0V)	KEYBOARD	4
29	+5V	KEYBOARD	5
31	GND (0V)	SERIAL	5
33	DTR	SERIAL	4
35	TXD	SERIAL	3
37	RXD	SERIAL	2
39	DCD	SERIAL	1
41	INTENSITY	VIDEO	6
43	VID. OUT	VIDEO	7
45	HSYNC	VIDEO	8
47	VSYNC	VIDEO	9
49	+5V	SPEAKER	-

J2 PIN	SIGNAL	CONNECTS TO: PERIPHERAL	P
2	AUTOFD-	CENTRONICS	
4	ERROR-	CENTRONICS	
6	INIT-	CENTRONICS	
8	SLCTIN-	CENTRONICS	
10	GND (0V)	CENTRONICS	
12	GND (0V)	CENTRONICS	
14	GND (0V)	CENTRONICS	
16	GND (0V)	CENTRONICS	
18	GND (0V)	CENTRONICS	
20	GND (0V)	CENTRONICS	
22	GND (0V)	CENTRONICS	
24	GND (0V)	CENTRONICS	
26	KCLK	KEYBOARD	
28	KDATA	KEYBOARD	
30	RESET-	KEYBOARD	
32	RI	SERIAL	
34	CTS	SERIAL	
36	RTS	SERIAL	
38	DSR	SERIAL	
40	GND (0V)	VIDEO	
42	GND (0V)	VIDEO	
44	RED	VIDEO	
46	GREEN	VIDEO	
48	BLUE	VIDEO	
50	AUDIO	SPEAKER	

TABLE F1 - PIN ASSIGNMENTS OF TOP CABLE

J2 PIN	SIGNAL	CONNECTS TO: PERIPHERAL	PIN	J2 PIN	SIGNAL	CONNECTS TO: PERIPHERAL	PIN
1	GND (0V)	POWER SUPPLY		2	GND (0V)	POWER SUPPLY	
3	GND (0V)	POWER SUPPLY		4	GND (0V)	POWER SUPPLY	
5	+5V	POWER SUPPLY		6	+5V	POWER SUPPLY	
7	+5V	POWER SUPPLY		8	+5v	POWER SUPPLY	
9	2DISKS-	FLOPPY DISK	1	10	HDS-	FLOPPY DISK	2
11	GND (0V)	FLOPPY DISK	3	12	N/C	FLOPPY DISK	4
13	GND (0V)	FLOPPY DISK	5	14	N/C	FLOPPY DISK	6
15	GND (0V)	FLOPPY DISK	7	16	INDEX-	FLOPPY DISK	8
17	GND (0V)	FLOPPY DISK	9	18	DS0-	FLOPPY DISK	10
19	GND (0V)	FLOPPY DISK	11	20	DS1-	FLOPPY DISK	12
21	GND (0V)	FLOPPY DISK	13	22	MOEN1-	FLOPPY DISK	14
23	GND (0V)	FLOPPY DISK	15	24	MOEN0-	FLOPPY DISK	16
25	GND (0V)	FLOPPY DISK	17	26	DIRC-	FLOPPY DISK	18
27	GND (0V)	FLOPPY DISK	19	28	STEP-	FLOPPY DISK	20
29	GND (0V)	FLOPPY DISK	21	30	WD-	FLOPPY DISK	22
31	GND (0V)	FLOPPY DISK	23	32	WE-	FLOPPY DISK	24
33	GND (0V)	FLOPPY DISK	25	34	TRK0-	FLOPPY DISK	26
35	GND (0V)	FLOPPY DISK	27	36	WP-	FLOPPY DISK	28
37	GND (0V)	FLOPPY DISK	29	38	RDD-	FLOPPY DISK	30
39	GND (0V)	FLOPPY DISK	31	40	HS-	FLOPPY DISK	32
41	GND (0V)	FLOPPY DISK	33	42	DCHG-	FLOPPY DISK	34
43	GND (0V)	POWER SUPPLY		44	GND (0V)	POWER SUPPLY	
45	GND (0V)	POWER SUPPLY		46	GND (0V)	POWER SUPPLY	
47	+5V	POWER SUPPLY		48	+5V	POWER SUPPLY	
49	+5V	POWER SUPPLY		50	+5V	POWER SUPPLY	

TABLE F2 - PIN ASSIGNMENTS OF BOTTOM CABLE

BUS CONNECTORS

The ECAT is factory configured to support connection either to the STEbus or to the PC bus.

The STEbus connector pin assignments conform to the STEbus specification (IEEE1000). A small number of pins are not used on the ECAT and so these pins are not connected.

The first 62 pins of the PC bus connector are compatible with the 62 pin PC bus, and the final two pins provide extra power connections. A small number of pins are not used on the ECAT, or are connected internally, so these pins are not connected.

Pin assignments are given in Table F3:

ROW A PIN	STEbus SIGNAL	ROW C PIN	STEbus SIGNAL
A32	GND	C32	GND
A31	VCC	C31	VCC
A30	N/C (-12V)	C30	N/C (+12V)
A29	SYSCLK*	C29	N/C (+VSTBY)
A28	N/C (BUSAK0*)	C28	N/C (BUSAK1*)
A27	N/C (BUSRQ0*)	C27	N/C (BUSRQ1*)
A26	GND	C26	ATNRQ7*
A25	ATNRQ6*	C25	ATNRQ5*
A24	ATNRQ4*	C24	ATNRQ3*
A23	ATNRQ2*	C23	ATNRQ1*
A22	ATNRQ0*	C22	SYSRST*
A21	TFRERR*	C21	GND
A20	DATACK*	C20	DATSTB*
A19	ADRSTB*	C19	GND
A18	CM2	C18	CM1
A17	CM0	C17	A19
A16	A18	C16	A17
A15	A16	C15	A15
A14	A14	C14	A13
A13	A12	C13	A11
A12	A10	C12	A9
A11	A8	C11	A7
A10	A6	C10	A5
A9	A4	C9	A3
A8	A2	C8	A1
A7	A0	C7	GND
A6	D6	C6	D7
A5	D4	C5	D5
A4	D2	C4	D3
A3	D0	C3	D1
A2	VCC	C2	VCC
A1	GND	C1	GND

TABLE F3 - STEbus PIN ASSIGNMENTS

Row A is the lower row (closest to the PCB) and row C is the upper row, when looking towards the DIN connector pins. Pin 1 is towards the bottom of the ECAT (near the battery).

ROW B PIN	PC bus SIGNAL	ROW A PIN	PC bus SIGNAL
B31	GND	A31	A0
B30	OSC	A30	A1
B29	VCC	A29	A2
B28	ALE	A28	A3
B27	TC	A27	A4
B26	-DACK2	A26	A5
B25	IRQ3	A25	A6
B24	N/C (IRQ4)	A24	A7
B23	IRQ5	A23	A8
B22	N/C (IRQ6)	A22	A9
B21	N/C (IRQ7)	A21	A10
B20	CLK	A20	A11
B19	-REFRESH	A19	A12
B18	DREQ1	A18	A13
B17	-DACK1	A17	A14
B16	DREQ3	A16	A15
B15	-DACK3	A15	A16
B14	-IORD	A14	A17
B13	-IOWR	A13	A18
B12	-MEMR	A12	A19
B11	-MEMW	A11	AEN
B10	GND	A10	IOCHRDY
B9	N/C (+12V)	A9	D0
B8	N/C (0 WAITS)	A8	D1
B7	N/C (-12V)	A7	D2
B6	DREQ2	A6	D3
B5	N/C (-5V)	A5	D4
B4	IRQ2	A4	D5
B3	VCC	A3	D6
B2	RESET	A2	D7
B1	GND	A1	-IOCHCK
B0	GND (Extra pin)	A0	VCC (Extra pin)

TABLE F4 - PC BUS PIN ASSIGNMENTS

Row A is the inner of the the rows on the pin header, and Row B is the row closest the edge of the ECAT PCB. Pin 31 is closest to the top of the PCB, near the two PALs. For clarity the two extra pins, which do not connect to the 62 pin edge connector on the PC bus cards, are called pins A0 and B0.

ECAT-X PERIPHERAL CONNECTORS

The ECAT-X has three connectors - two for video and one for the COM2: serial port. These are arranged as two 10 way headers and one 16 way header. If required these three connectors can be replaced by a single 50 way connector, with cable retaining latches, and the 50 way ribbon cable can be split and directed to the peripherals as required.

PIN	SIGNAL	CONNECTS TO FEMALE 15-WAY HIGH-DENSITY D-TYPE PIN:	CONNECTS TO FEMALE 9-WAY D-TYPE PIN:
1	GND	6	6
2	RED	1	1
3	MS0	11	-
4	GND	7	7
5	GREEN	2	2
6	MS1	12	-
7	GND	8	3
8	BLUE	3	8
9	HSYNC	13	4
10	N/C	9	-
11	MS2	4	-
12	VSYNC	14	5
13	GND	10	9
14	GND	5	-
15	N/C	15	-
16	N/C	-	-

TABLE F5 - PIN ASSIGNMENTS FOR VGA GRAPHICS PORT (J4)

Note: The 15 way connector is the IBM standard. It is a 15 way connector with three rows of pins in a headshell the same size as a standard 9-way D-type. The 9 way connector is a standard 9-way D-type. The pin assignments are those used by some monitor manufacturers, including Quadram.

PIN	SIGNAL	CONNECTS TO FEMALE 9-WAY D-TYPE PIN:
1	GND	1
2	INTENSITY	6
3	GND	2
4	MONO VIDEO	7
5	RED	3
6	HSYNC	8
7	GREEN	4
8	VSYNC	9
9	BLUE	5
10	GND	-

TABLE F6 - PIN ASSIGNMENTS FOR EGA/MONO GRAPHICS PORT (J5)

PIN	SIGNAL	DIRECTION	CONNECTS TO MALE 9-WAY D-TYPE PIN:
1	DCD	INPUT	1
2	DSR	INPUT	6
3	RxD	INPUT	2
4	RTS	OUTPUT	7
5	TxD	OUTPUT	3
6	CTS	INPUT	8
7	DTR	OUTPUT	4
8	RI	INPUT	9
9	GND	-	5
10	GND	-	-

TABLE F7 - PIN ASSIGNMENTS FOR COM2: SERIAL PORT (J3)

APPENDIX G INTRODUCTION TO THE STEbus

The following pages are extracted from a leaflet published by the STEbus Manufacturers and Users Group. It gives an overview of the STEbus for those ECAT users who may not have met it.

FROM
THE STE MANUFACTURERS
AND USERS GROUP

Now approved as a full standard by the Institute of Electrical and Electronic Engineers

STEbus

IEEE 1000 *standard*

Designed by Engineers for Engineers

"The only truly manufacturer-independent 8-bit bus"

- Manufacturer independent – widest processor choice of any 8-bit bus
- Performance into the future – asynchronous, non-multiplexed data transfers at over 5 Mbytes/sec
- Full 1 Mbyte addressing range
- Extensive I/O capability – up to 4 kbytes of I/O space
- Position independent, non-daisychained bus
- Designed as a low-cost – 8-bit bus embracing Eurocard standard
- Multiprocessing capability
- High speed burst transfer mode
- Eight attention request lines
- Vectored or non-vectored interrupts
- Interrupt acknowledge cycle
- Read modify-write cycle
- Designed for high data integrity. Fully buffered signals, terminated backplane

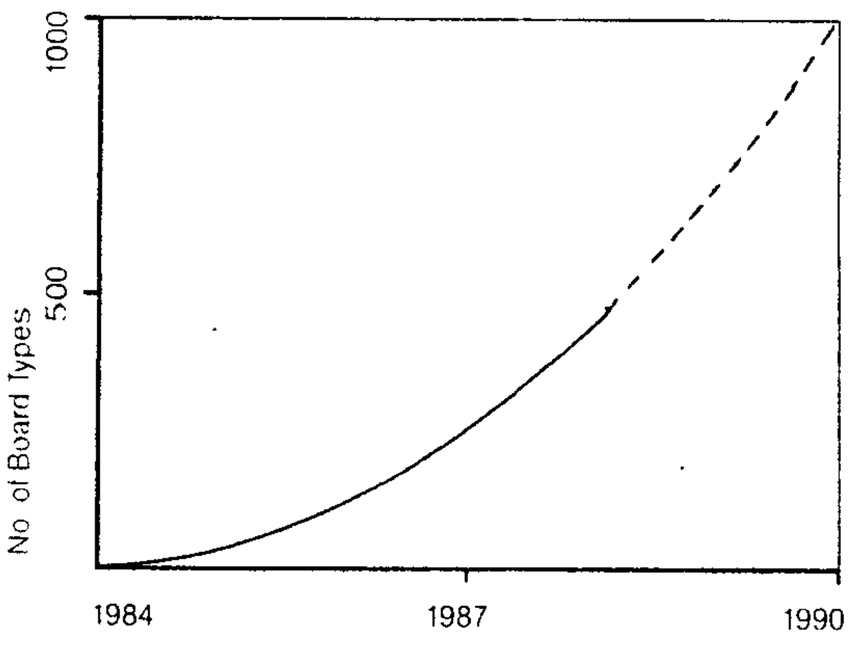


Figure 1: In less than four years the STEbus has become a major international bus standard. There are now over 700 board types available to system integrators and over 50 suppliers of STEbus products worldwide.

The Origins Of STEbus

STEbus was created in 1982 when the Institute of Electrical and Electronic Engineers in the US, the international standard makers for bus systems, set up a working group to develop it. The term STEbus was coined from visions of a Eurocard version of the STD bus, the then dominant 8-bit standard.

The end result was, however, very different. Taking full account of the latest trends in processor and system design, the working group created a totally new low-cost 8-bit bus to meet the needs of today's designers – and those of tomorrow.

The major buses of the early eighties were closely associated with particular manufacturers and had become, through their popularity, essentially de facto standards. STEbus broke new ground as the first bus system to be created independently of commercial interests. It was designed by engineers for engineers.

Since the specification was agreed in 1984, the number of STEbus boards and suppliers has mushroomed (figure 1). The STEbus now has a major following and is easily the fastest growing 8-bit bus. Support for STEbus is highest in the UK where most of the pioneering work was done, but the bus is also rapidly gaining popularity in both Europe and the US.

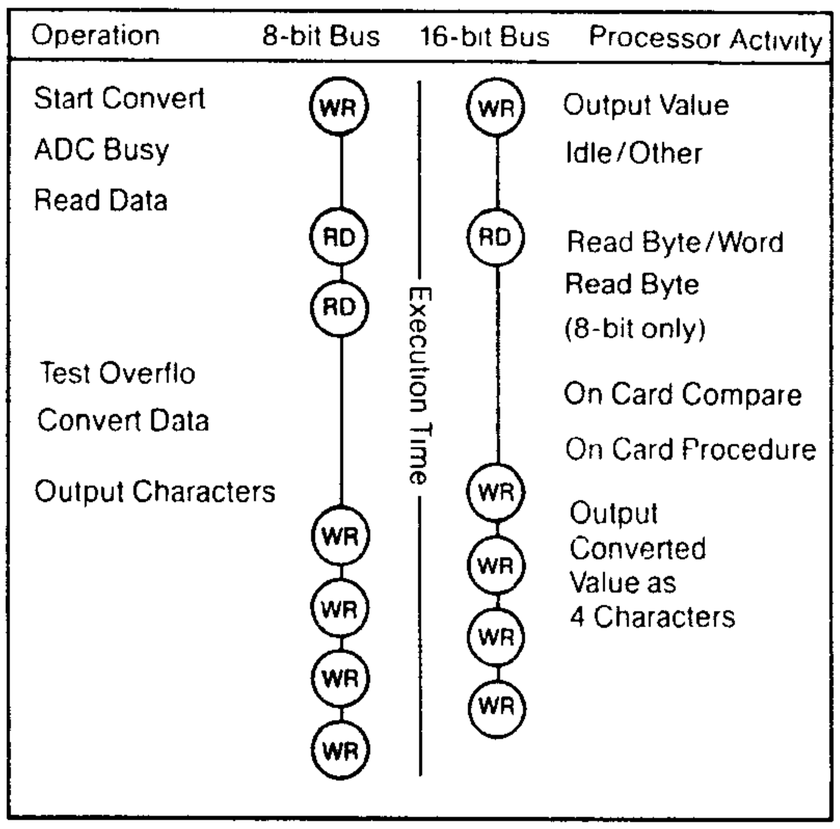


Figure 2: There can be little advantage in using wide buses for I/O in control and instrumentation systems. In the data path for an average speed 12-bit ADC to a logging device, the only gain apparent from using the 16-bit bus is a reduction in time of one Read cycle.

Why Another Eight-Bit Bus?

By the early eighties, backplane buses such as STD which were developed in the mid-seventies were already showing their age. Such trends as faster processors, wider addressing ranges, CMOS and multiprocessing were slowly making them obsolete. Only limited upgrades were possible while maintaining compatibility with boards produced to the original standard. STEbus's creators saw the need for a next generation bus.

Though processors were gradually moving up in complexity from 8- to 16- to 32-bits, a conscious decision was made during STEbus's development to restrict data transfers to 8 bits, and 8 bits only. There was one simple reason for this – cost. The added complexity of allowing wider data paths would have significantly increased the cost of each STEbus board and reduced the board area available for useful functions.

Within its class, STEbus nonetheless offers high performance, allowing data to be transferred at over 5 Mbytes/sec. Since 8-bit versions of popular 16- and even 32-bit processors are widely available, the STEbus user is not restricted to older processor technology.

In such fields as industrial control, 8-bit computing is, and will remain, perfectly suitable for most systems (figure 2). Though engineers who want powerful number-crunching systems would be better advised to look to a 32-bit bus standard such as VME or Futurebus, they could also benefit from STEbus as an I/O bus (figure 3).

It is easy for a 16-bit or 32-bit bus to become I/O bound since most interface standards to industrial computers are byte organised – SASI, SCSI, IEEE 488 and RS232 for example. Data must often be transferred between a peripheral device and the CPU a byte at a time, wasting ¾ of the bus bandwidth in a 32-bit system. In contrast, STEbus can make full use of its bus.

STEbus's 8-bit bus also avoids the problems faced by 32-bit systems in coping with the different ways various microprocessors justify data bytes. Byte swapping logic is unnecessary and this, coupled with far fewer transceiver and control components, leads to an interface that is easy to implement and inexpensive.

The simplicity of the interface means significant savings over 16-bit and 32-bit systems in both the design time and production cost of any custom boards that are made. It also allows a relatively small board size. STEbus is defined as single or double Eurocard, though single height boards are more common.

A small board size also helps keep costs low through less expensive packaging and reduced granularity. Designers are more likely to be able to configure precisely the functions they require if there are fewer per board.

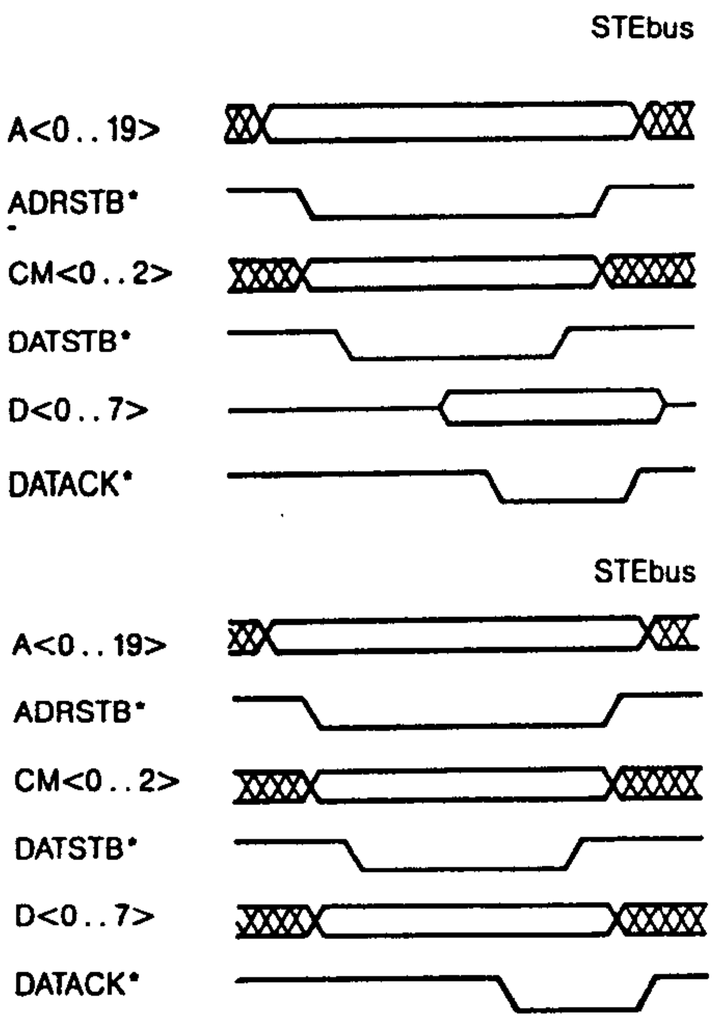


Figure 5: Read and Write cycles for the STEbus. In the Read cycle the address bus is driven by the master and qualified by ADRSTB*. The command bus is then driven by the master and qualified by DATSTB*. Finally, the slave drives the data bus and the DATACK* handshake line when the data is valid. The Write cycle proceeds in similar fashion.

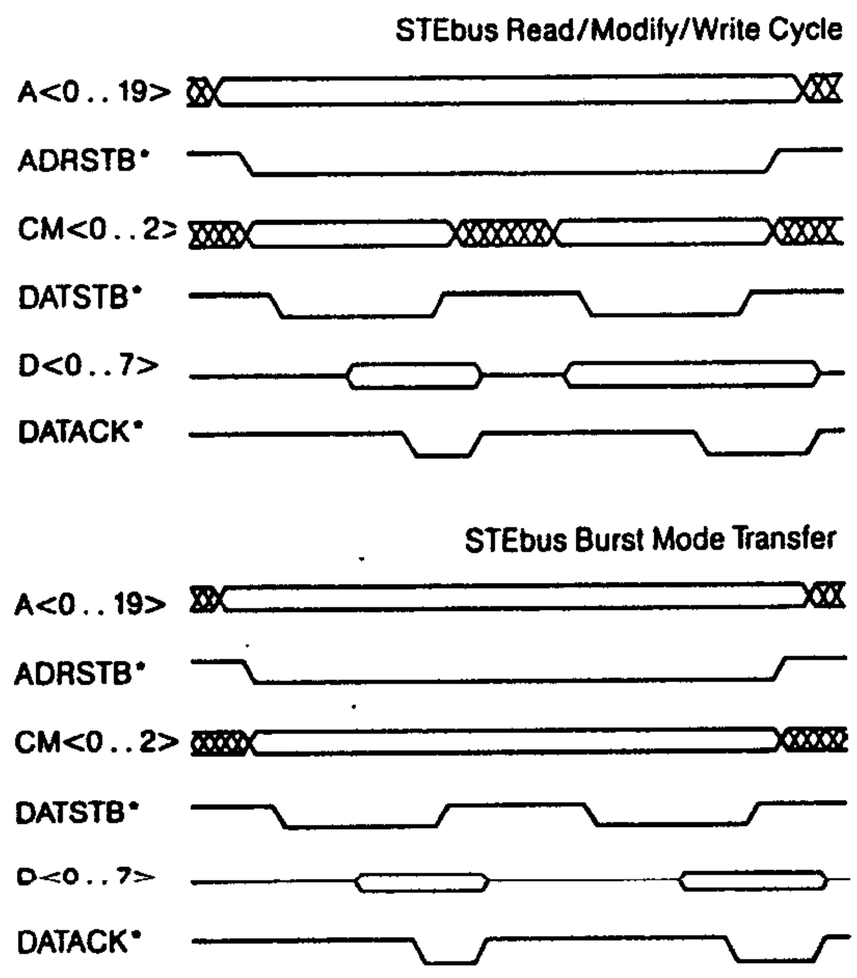


Figure 6: The STEbus Read/Modify/Write cycle and Burst Mode Transfer. In the Read/Modify/Write cycle, the master holds the address lines stable but changes the command bus. Two handshake sequences – first the read cycle then the write cycle – are performed. In the Burst Mode Transfer, the slave performs the first access at the address supplied by the master. The master holds the address constant for subsequent cycles while the slave increments the address.

Why Eurocard?

Almost all the more recent buses have adopted the Eurocard form factor, and this standardisation on board sizes is a major boon to the system designer. Eurocard mounting hardware is readily and cheaply available from many sources, as are such items as prototyping boards, power supplies, modem cards and networking hardware.

Apart from offering the widest choice, Eurocard allows engineers to maximise the use of enclosure space and ancillaries such as power supplies while reducing costs by including a variety of functions, whether related or not, within the same box. The unique connectors and board sizes used by the older buses have become their Achilles heel as more engineers insist on using the Eurocard format.

How Long Will STEbus Last?

Recognising that a backplane bus represents a major investment, great care was taken in developing the specification to give STEbus as long a life as possible. Building-in such advanced features as processor independence and multiprocessor capability were key to this philosophy, as was the generous allocation of address and I/O space.

Just as fundamental, however, was the choice of data transfer protocol. Older buses were commonly synchronous, so their maximum performance was limited at their inception, allowing little room for speed improvements as device technology improved. Like other modern buses such as VMEbus and Futurebus, STEbus overcomes this problem by employing an asynchronous handshake protocol.

With such a system, the speed of data transfer is governed by the slowest participating board, and not by timing figures in the specification. This allows the possibility of performance improvements as and when faster devices can be used. Also, STEbus's protocol does not unduly favour any particular processor family, thereby giving the designer a wide choice of CPU and facilitating the mixing of processor types in a multiprocessor system.

How Does STEbus Handle Interrupts?

The STEbus allows interrupts to be processed in several ways. At the simplest level, for such interrupts as Power Fail, no acknowledge is necessary and an ATNRQn* line is asserted by the interrupting module. For 'common' interrupts, the interrupting module is acknowledged by a read or write operation on one of its registers.

Bus-vectored interrupts are the most powerful. In these, an interrupt handler uses the bus's command modifier lines to indicate an acknowledge cycle and puts the encoded ATNRQn* line number onto the address bus as a 3-bit address. The interrupting module can then put an interrupt vector onto the bus which the handler reads in the acknowledge cycle.

How Is Priority Determined?

Unlike a number of other buses that use daisychaining and hence impose device dependent timing constraints, STEbus allows boards to be placed anywhere along the backplane. Priority is determined by which of the eight Attention Request (ATNRQn*) lines a board asserts. ATNRQ0* holds highest priority, ATNRQ7* the least. The position independence of STEbus boards facilitates system building and servicing and is a far more flexible solution for generating interrupts.

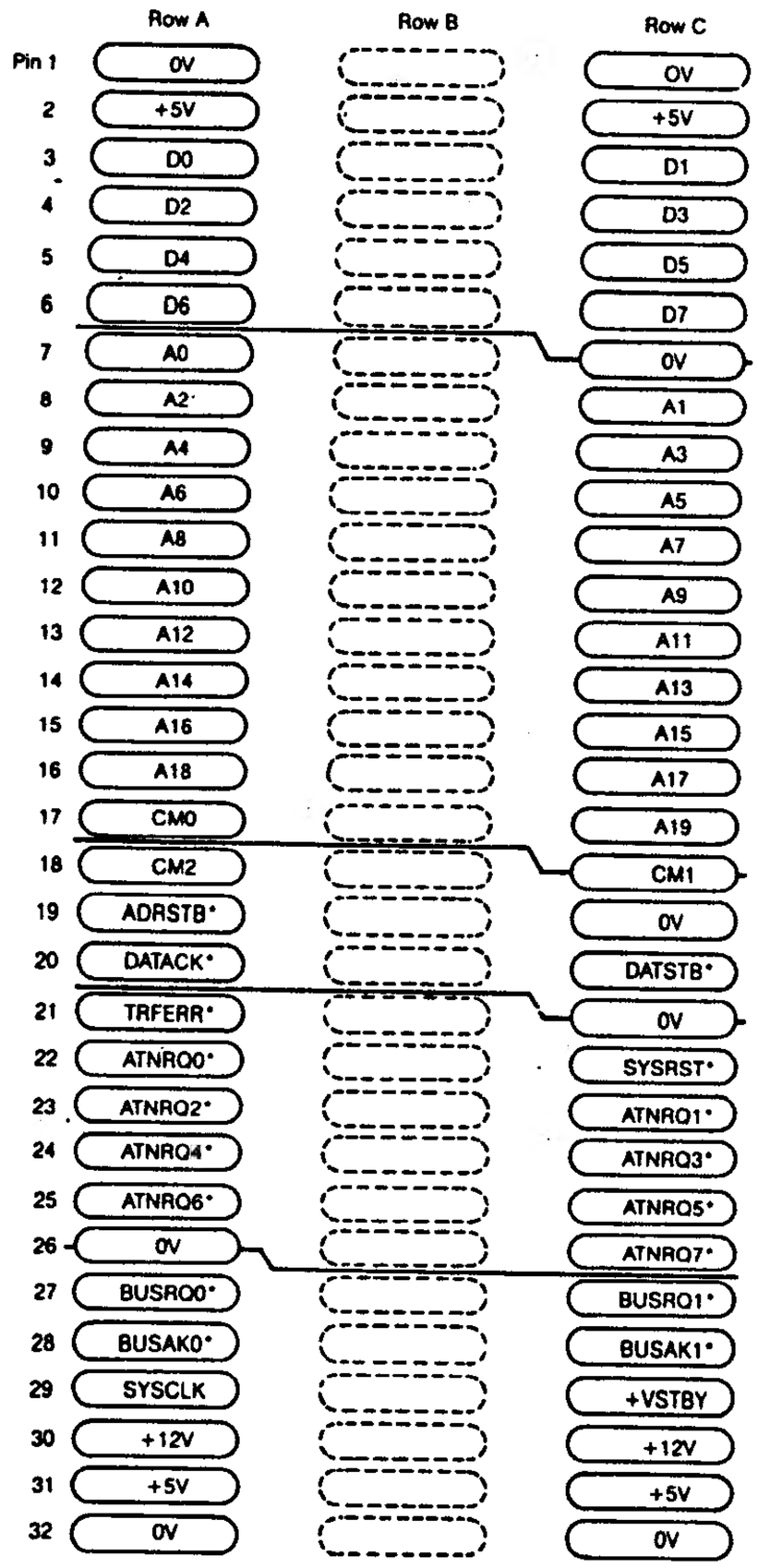


Figure 7: The 64-signal STEbus pin-out defined on rows A and C of a DIN 41612 connector. Address lines A0-19 provide 1 Mbyte of main memory addressing. Depending on the cycle, A0-11 are used to address the 4 kbytes of I/O space and A0-2 provide a 3/bit acknowledge address. Lines D0-7 are the 8-bit data bus. ADRSTB* and DATSTB* are address and data strobes. Lines CM0-2 define the type of bus cycle in progress (whether memory or I/O read or write or an acknowledge). Request lines BUSRQ0,1* are used by temporary masters. DATACK* is asserted when a master accepts data (on a read cycle) or when data is valid (on a write cycle). TRFERR* is used if data from a slave is incorrect. Signals ATNRQ0-7* are attention request lines and SYSCLK* and SYSRST* are for a 16 MHz clock and reset functions. The remaining lines are for power and fully distributed grounds.

What About Future Upgrades?

The in-built compatibilities between STEbus and VME reflect an unstated objective of the STEbus working group – that both physical and conceptual upwards migration paths from STEbus to VME should be provided to allow systems engineers to maintain their investment in STEbus when developing more powerful, next generation systems.

Coupler boards which link STEbus bus subsystems to VME are available. Using these, a large portion of an existing STEbus system can literally be grafted onto the new VMEbus based system. With an intelligent interface, the existing software can also be used.

Can STEbus Operate In Harsh Environments?

The STEbus is designed to be as tolerant as possible to harsh environments. By adopting the Eurocard format, STEbus uses the highly reliable two-part DIN 41612 connector, a great improvement on the direct edge connectors used by older bus standards. All signal lines are buffered and the backplane properly terminated.

A system error signal is also provided to further ensure the integrity of data transfers. This is asserted by the system controller if an acknowledge is not returned within a given time or by a slave if a local error occurs during a transfer. Crosstalk is minimised by the careful layout of signal lines on the DIN 41612 connector.

Who Is Using STEbus?

The STEbus has become widely used across industry – from communications and laboratory measurements through to machine and process control. In many cases, it is taking over the role of STD as a low-cost industrial bus. STEbus is also creating new markets. Companies are, for example, finding it better to build their own programmable logic controllers from STEbus boards rather than use inflexible ready-made PLC's.

With its advanced features and ability to use the latest processors, the STEbus is also proving popular in less demanding information processing applications in preference to a higher performance 32-bit bus such as VME. Generally, if STEbus can do the job, and system engineers resist the temptation to overspecify, they can build their systems at a fraction of the cost.

Is The STEbus Specification Fully Approved?

Yes. In December 1987, STEbus finally gained full IEEE approval. It is now known as IEEE 1000-1987 standard.

APPENDIX H FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a "Product Fault Report" form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form with the goods to your dealer.

Prior to returning a faulty product, please check the following:

1. The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the rack are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION

COMPANY NAME:

INDIVIDUAL CONTACT:

PHONE NO:

PRODUCT INFORMATION

PRODUCT/DOCUMENT:

SERIAL NO:

DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC)?

****

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT:

CHARGES TO BE INVOICED: £

DATE OF RETURN:

REPAIRED BY:

RETURNED BY: